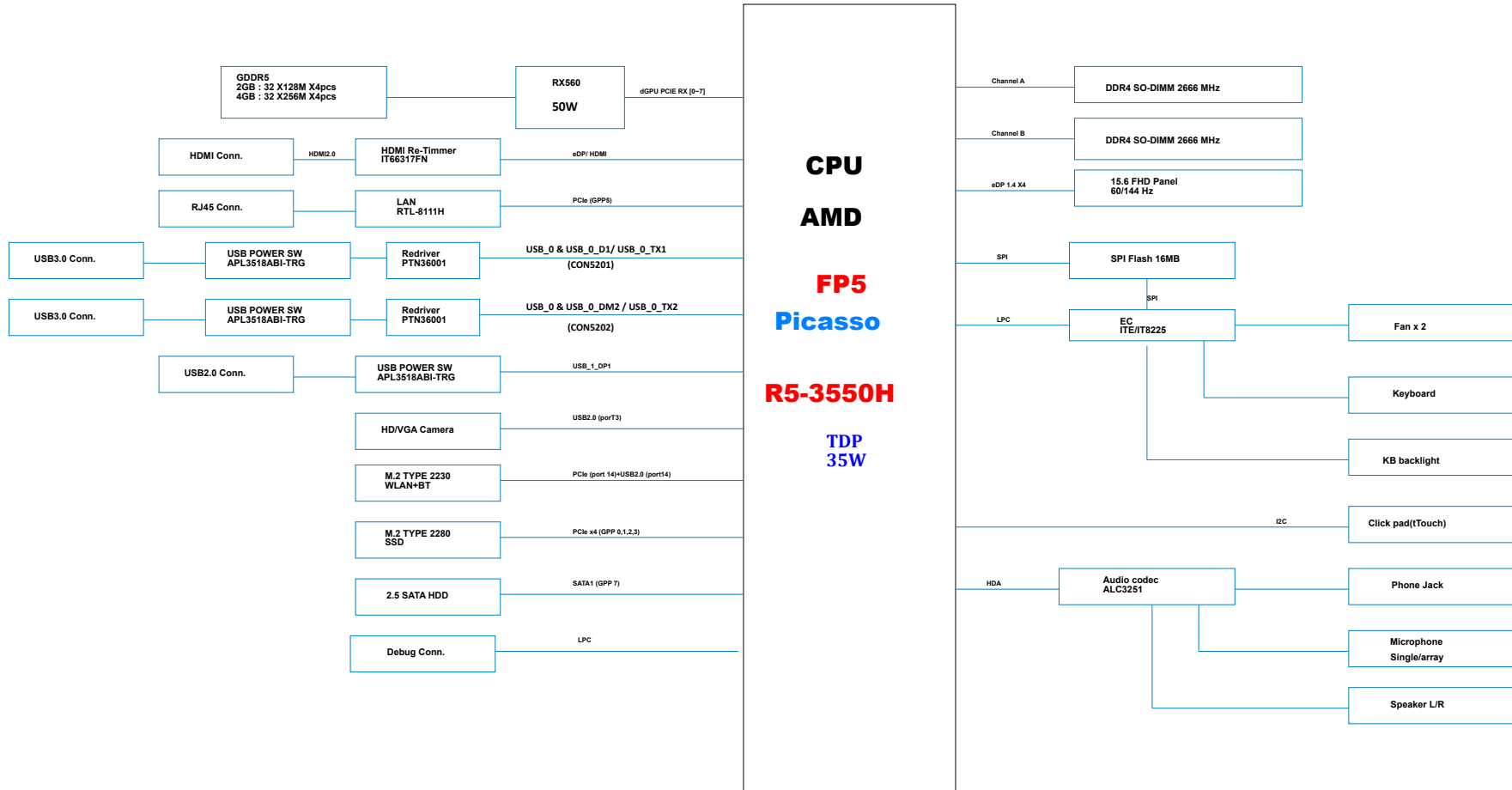


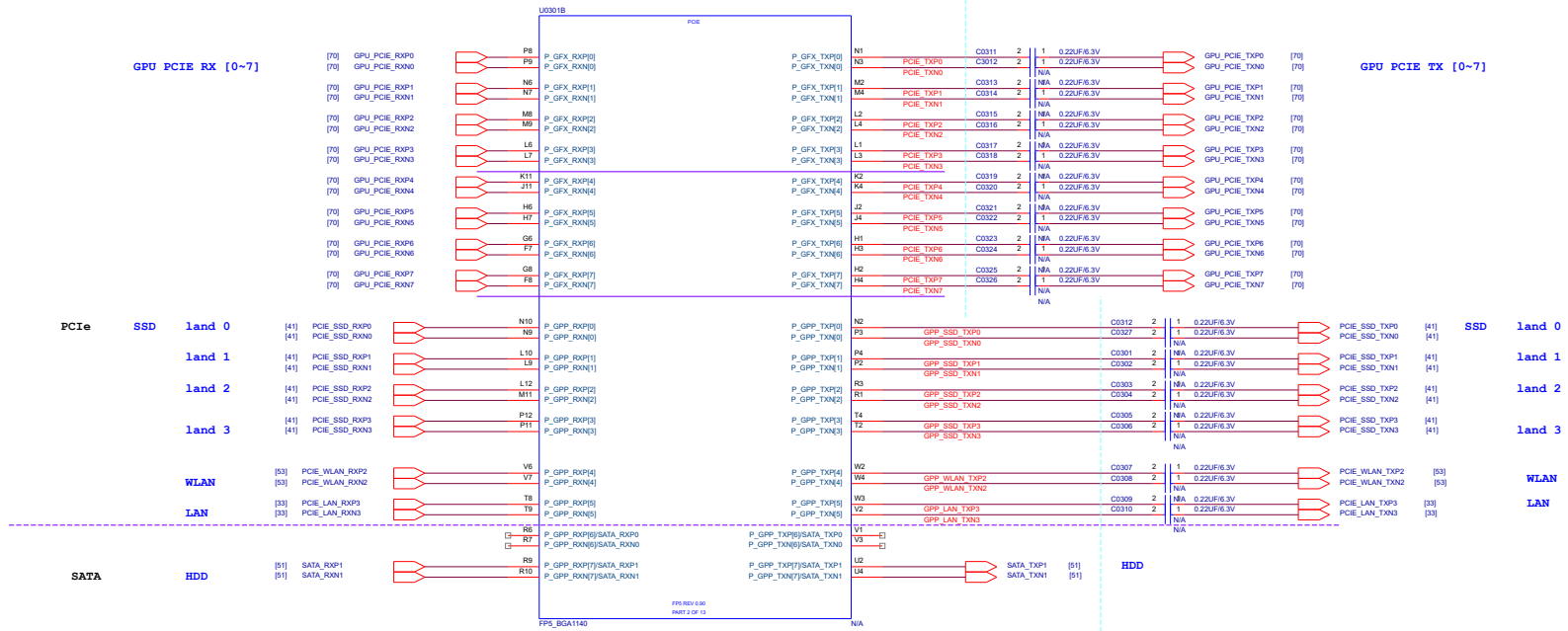
FX505DY AMD Block Diagram

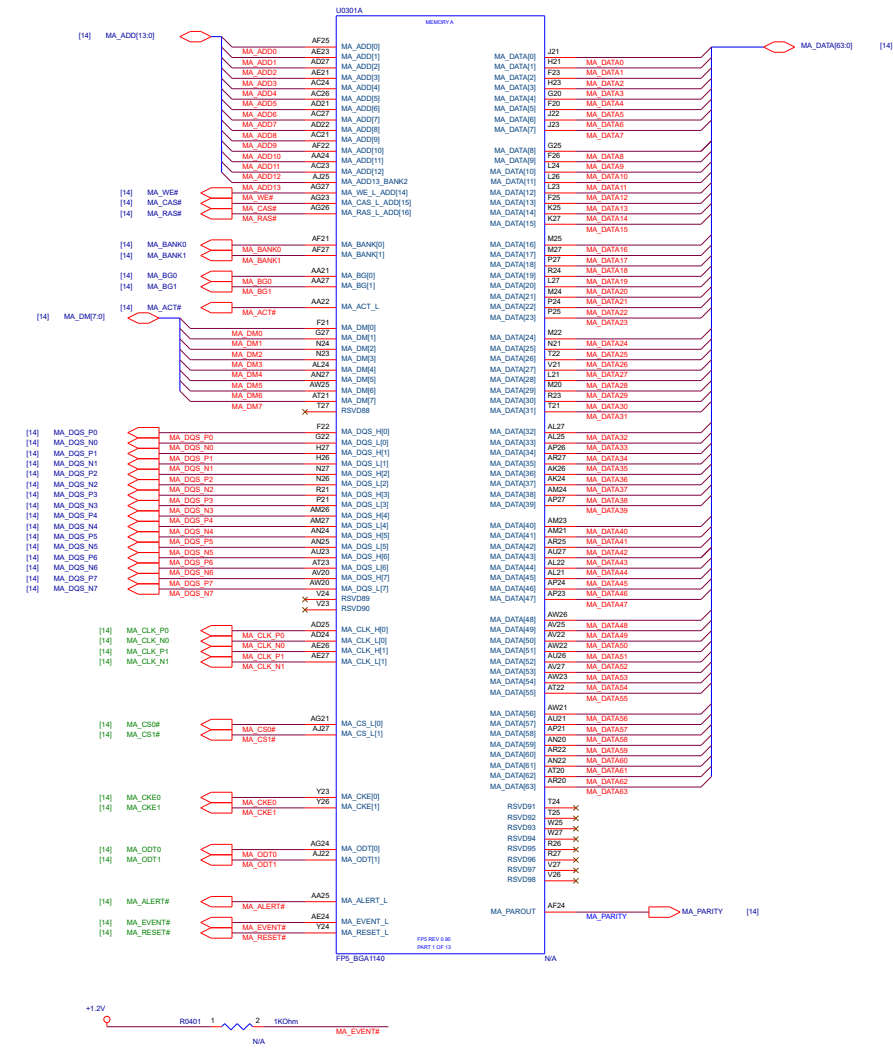
before PR3: PICASSO R5 3500H
After PR3: PICASSO R5 3550H



RX Side

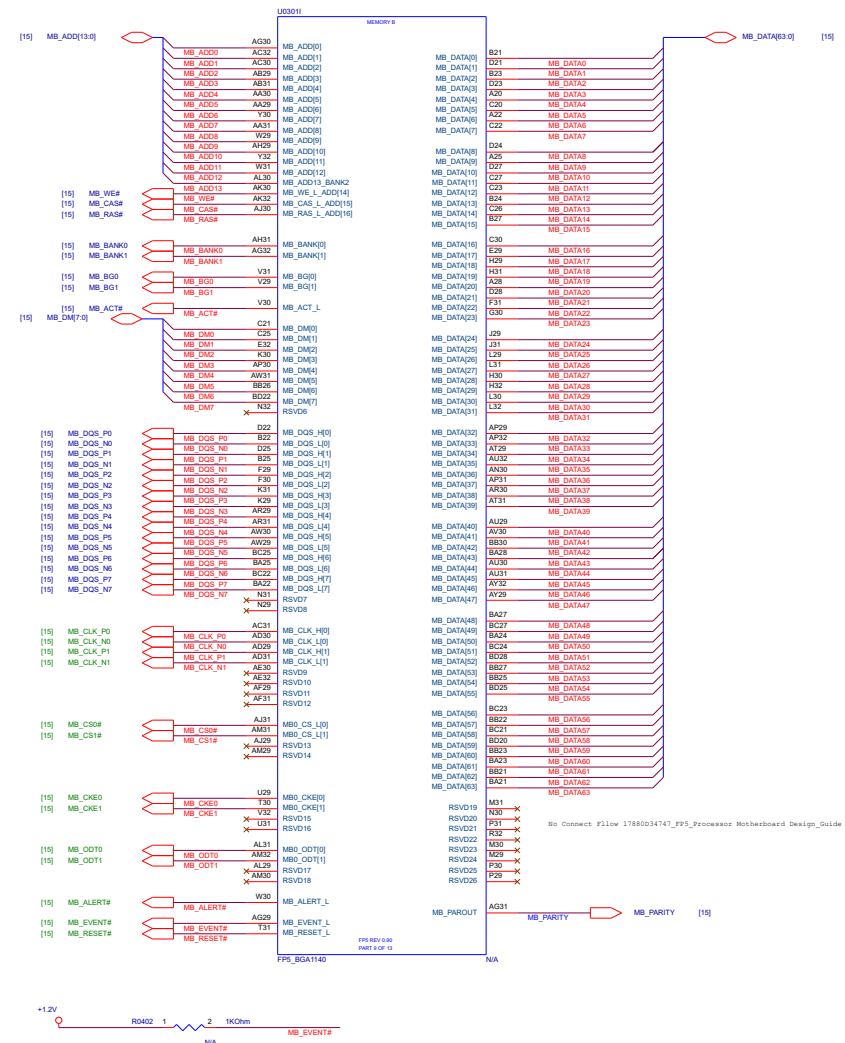
TX Side



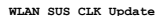
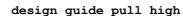
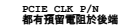


Memory Channel B

拉線OK, 有幾Pin訊號待確認是否會使用到

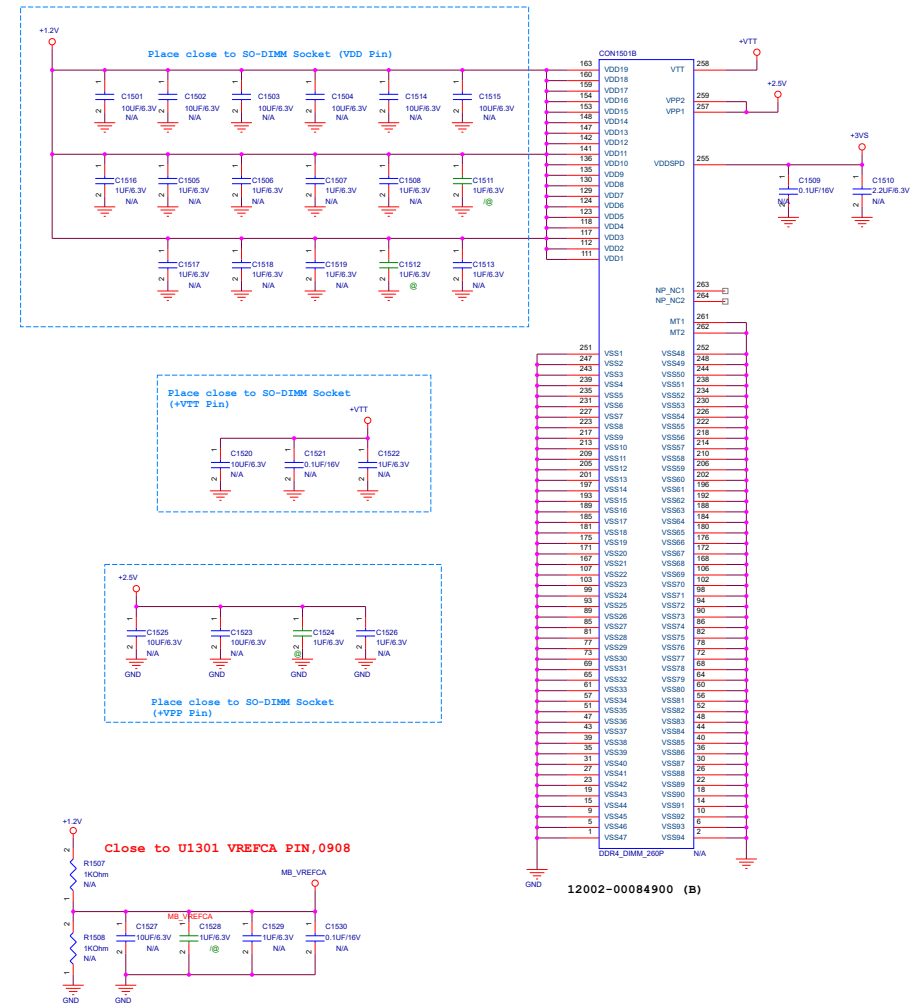
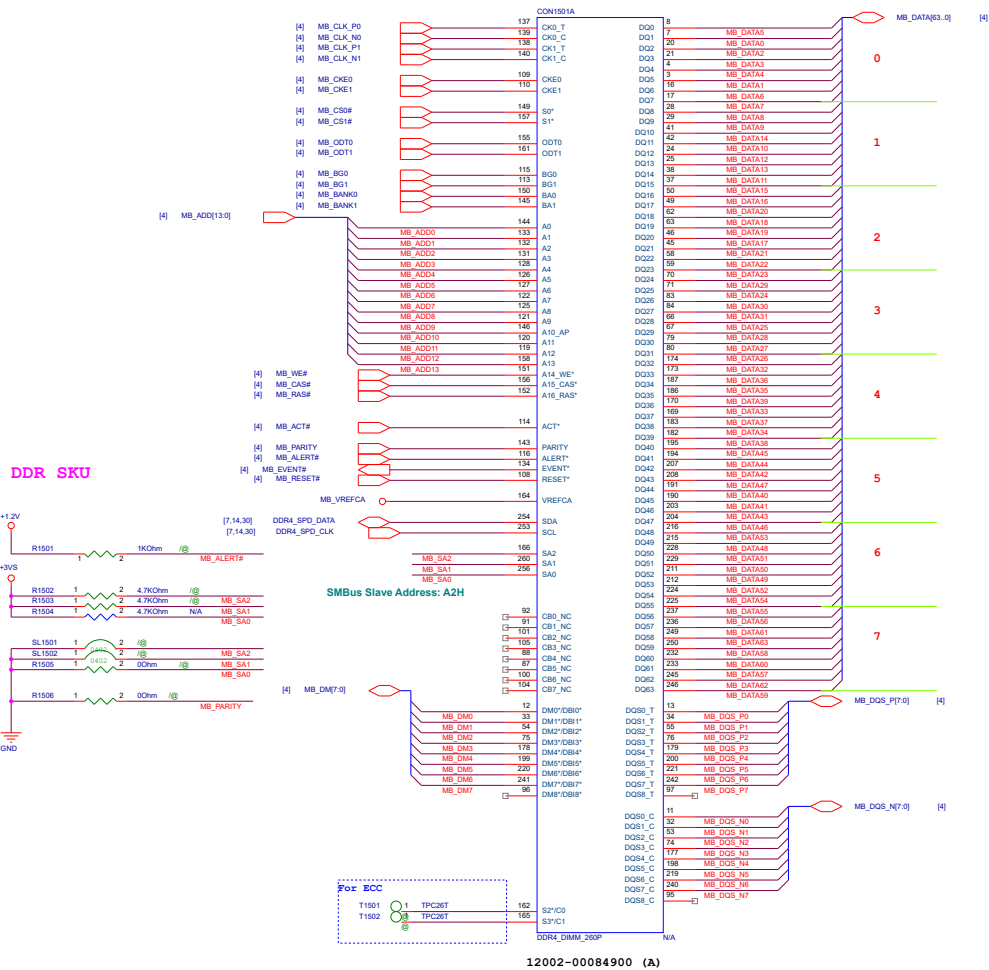


CPU CLK

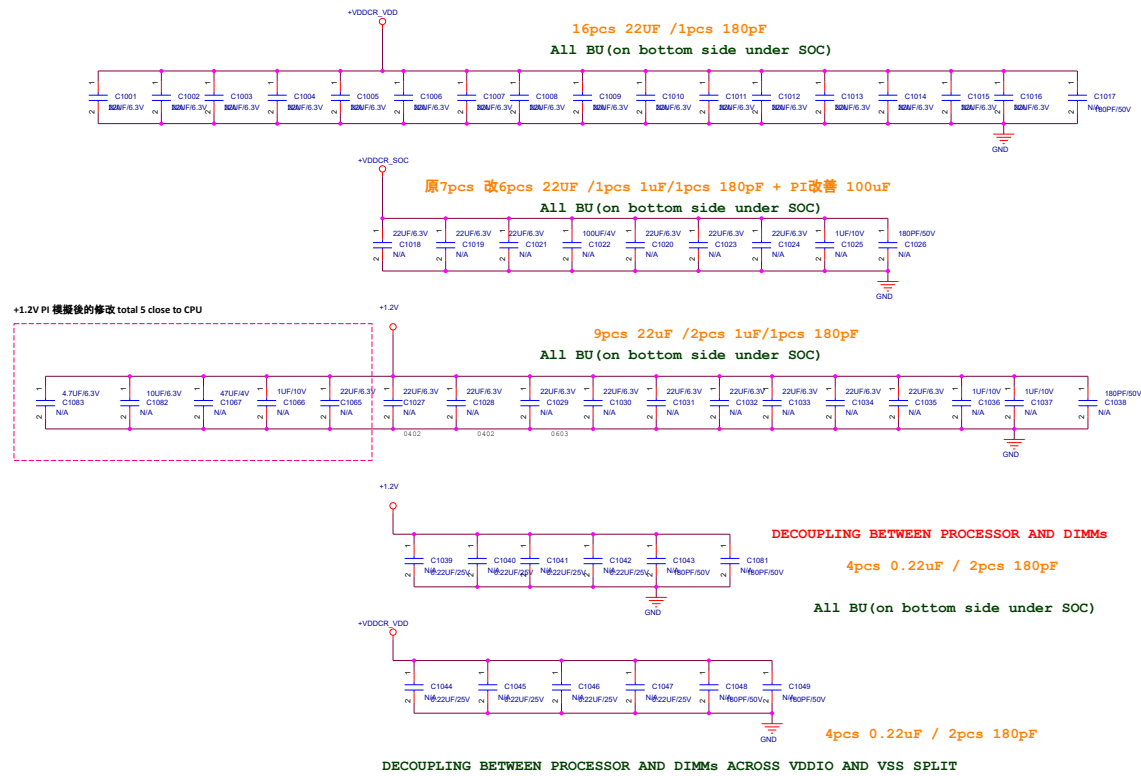




DDR4 SO-DIMM B rev 12002-00084900 5.2H STD

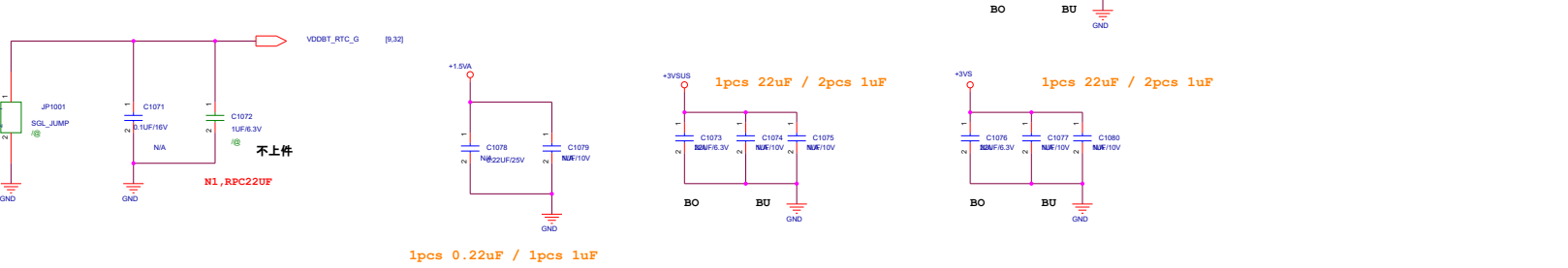


CPU_CAP

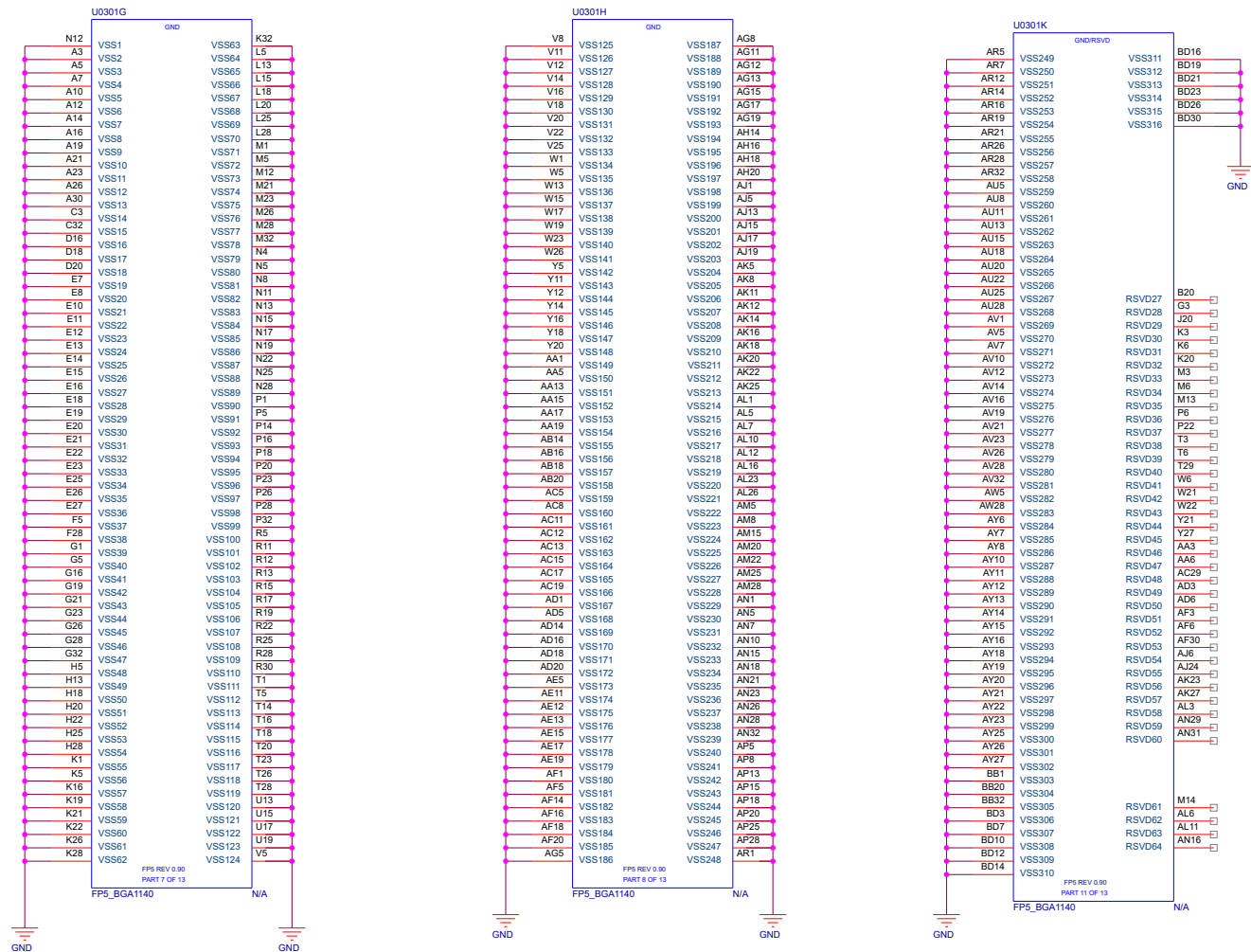


If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

POWER RAIL			
CPU	CPU_FP5	FX505ZD	CRB線路
Power rail	VDDCR_SOC	+VDDCR_SOC	+APU_VDDSOC_RUN
	VDDIO_MEM_S3	+1.2V	+APU_VDDIO_SUS
	VDDIO_AUDIO	+1.8VS	+VDD_AUD_ALW
	VDD_33	+3VS	+3.3V_RUN
	VDD_18	+1.8VS	+1.8V_RUN
	VDD_18_S5	+1.8VSUS	+1.8V_ALW
	VDD_33_S5	+3VSUS	+3.3V_ALW
	VDDP_S5	+0.9VSUS	+VDDP_ALW
	VDDP	+0.9VS	+VDDP_RUN
	VDDBT_RTC	+1.5VA	+VDDBT_RTC
	VDDCR	+VDDCR_VDD	+APU_VDDCORE_RUN



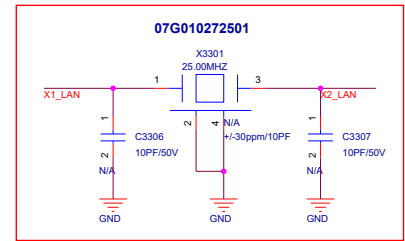
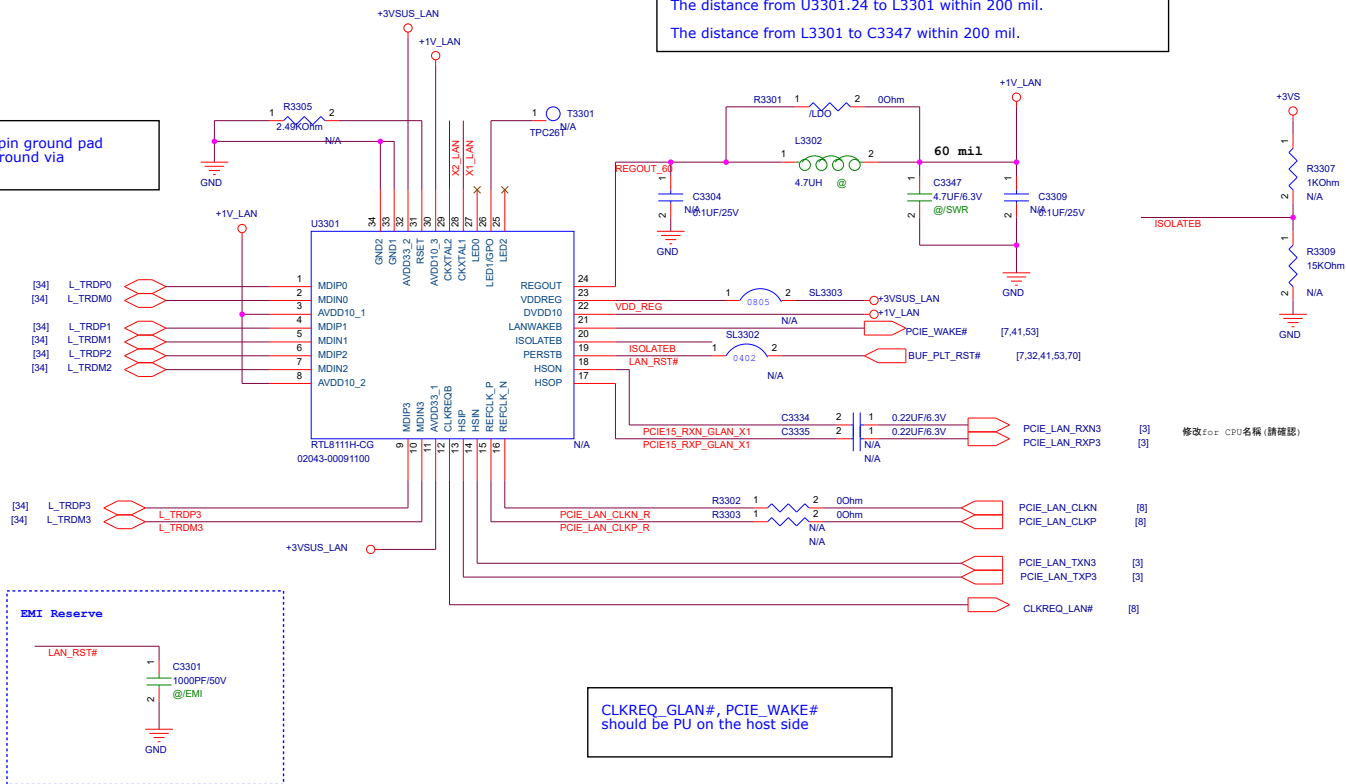
CPU_GND



The distance from U3301.24 to L3301 within 200 mil.

The distance from L3301 to C3347 within 200 mil.

33/34 pin ground pad
need ground via



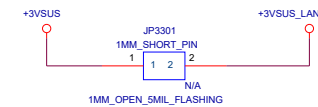
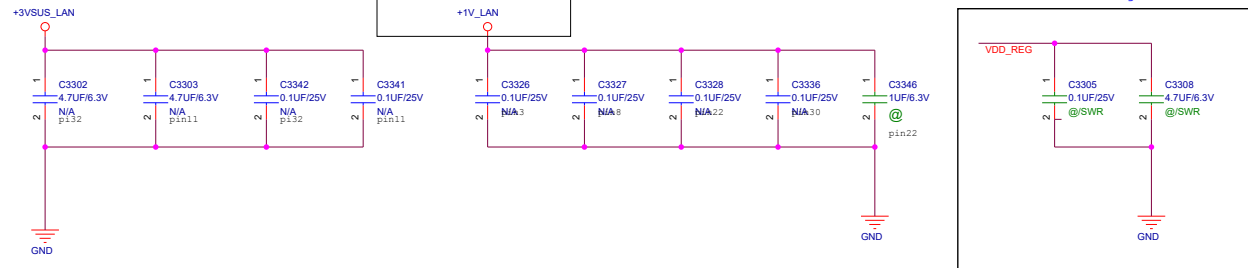
X3301: 25MHZ +/-30ppm/10pF (3225)

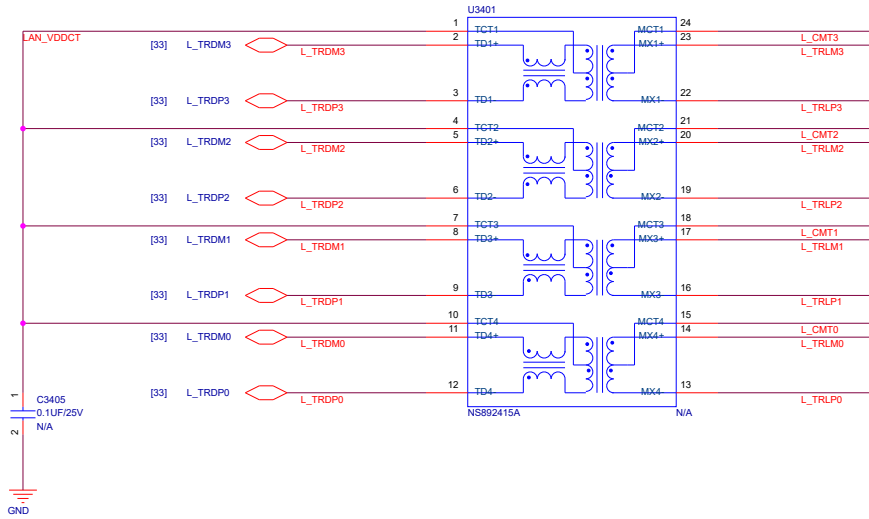
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

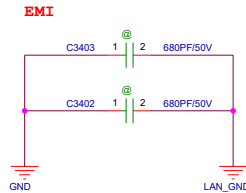
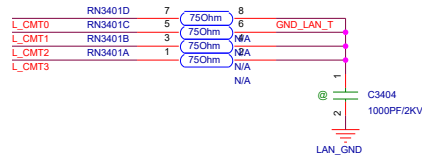
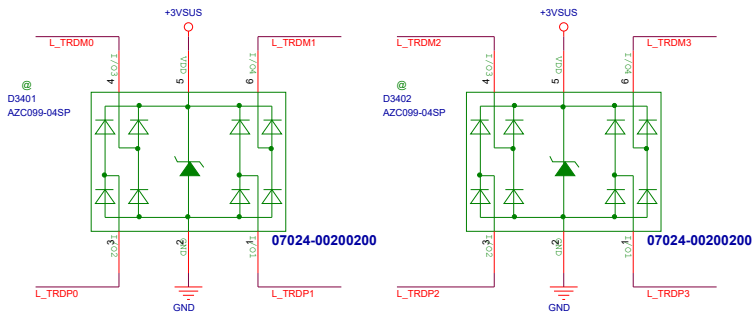
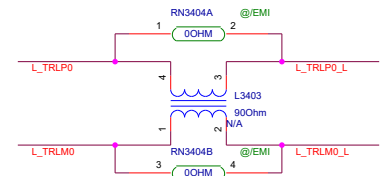
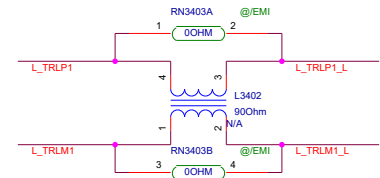
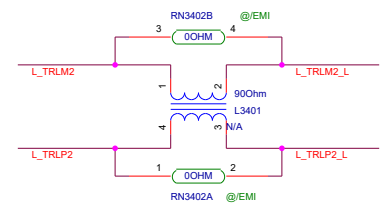
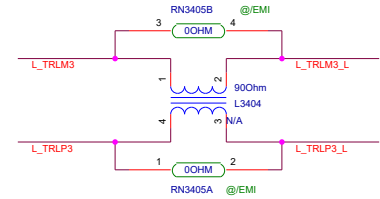
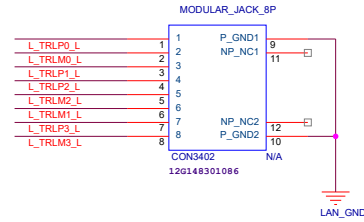
LAN 1V的電? 要確認由誰給的

20170913 Remove for NOT using SWR mode.





LAN Connector



Place near chassis GND

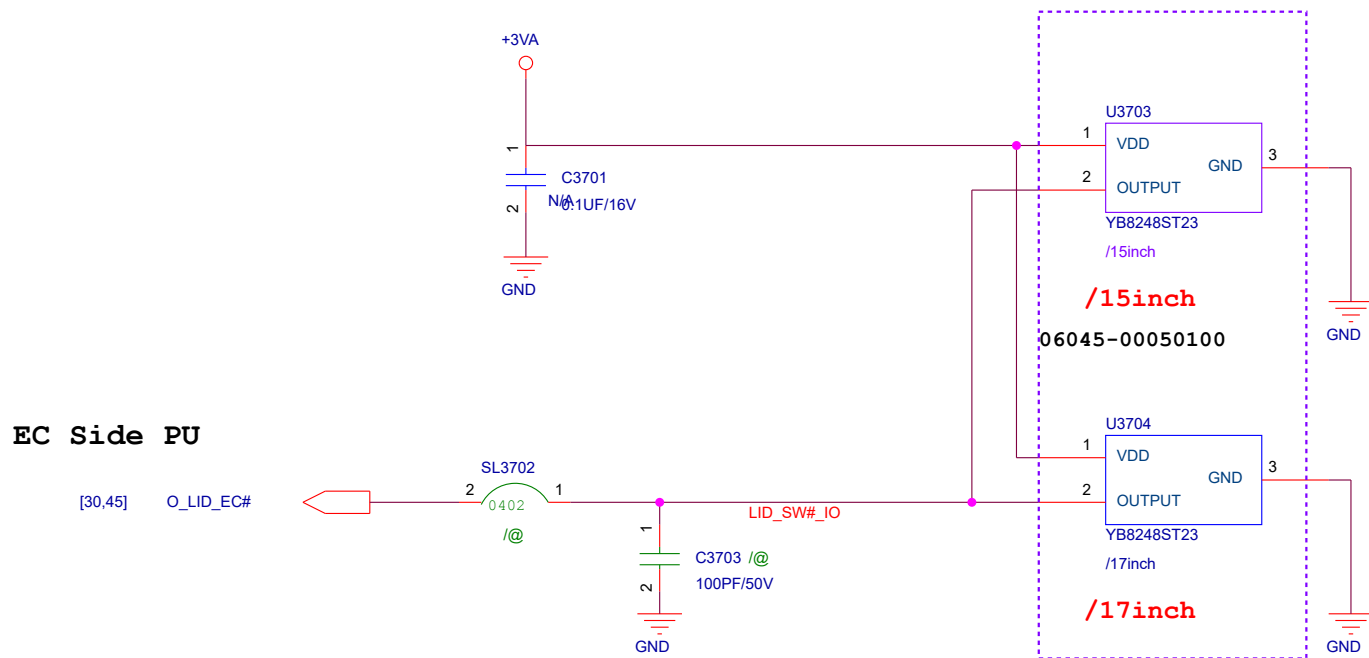
GND_LAN_T 上禁止加任何零件

D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

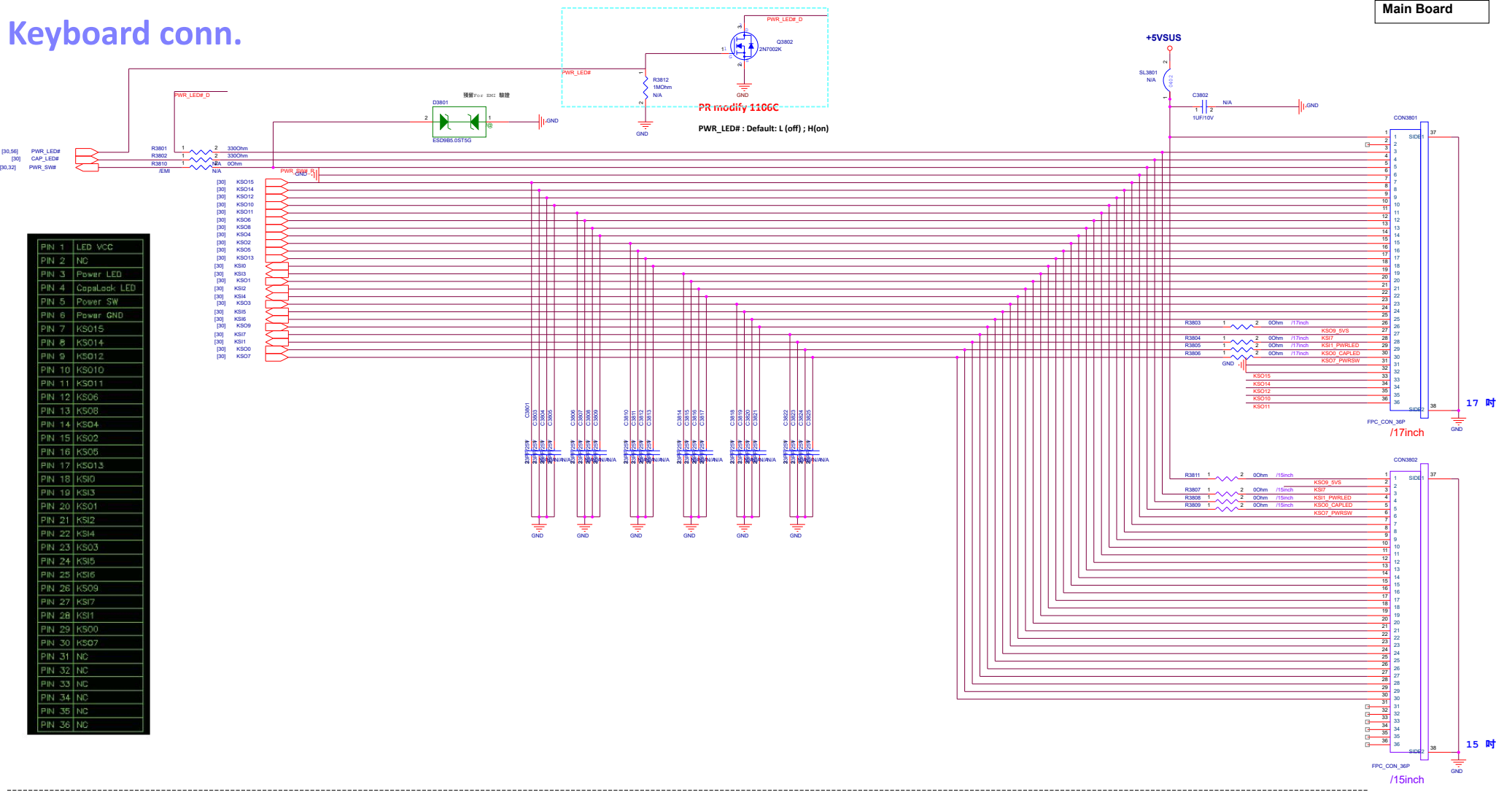
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

Hall Sensor



06033-00010000 另一顆料，互為替代料，目前沒3D Drawing

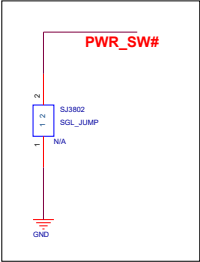
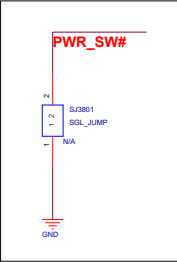
Keyboard conn.



Power-on jumper

請放置於空曠處 (TOP)

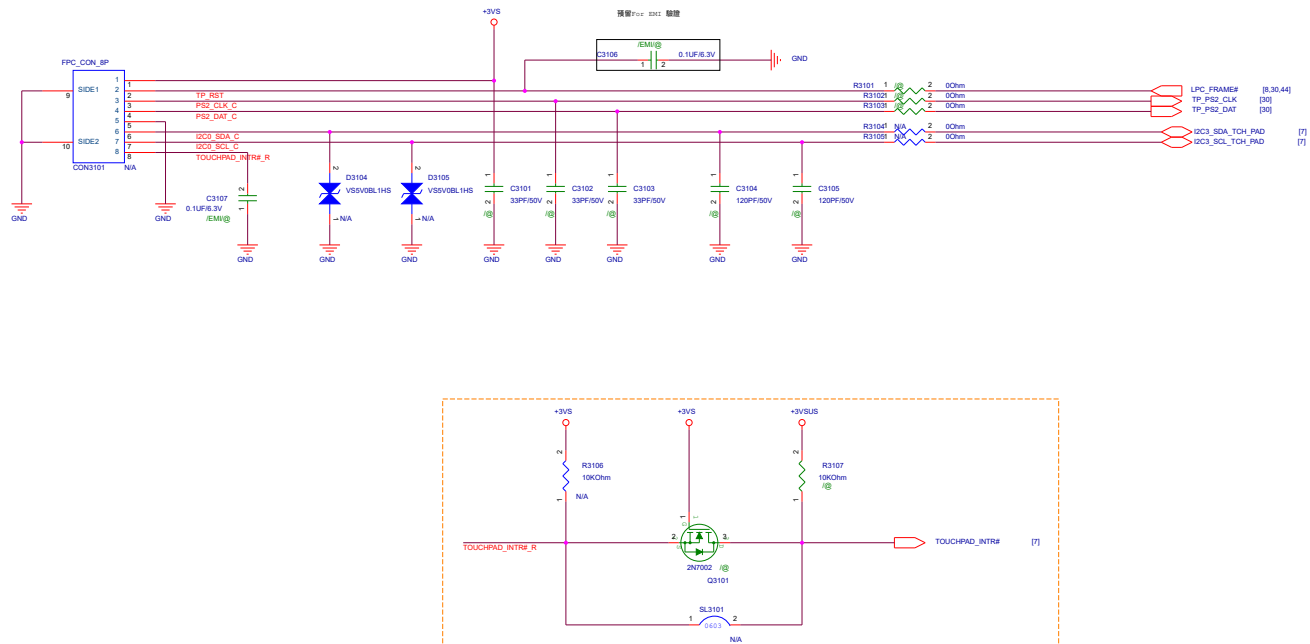
請放置於空曠處 (BOTTOM)



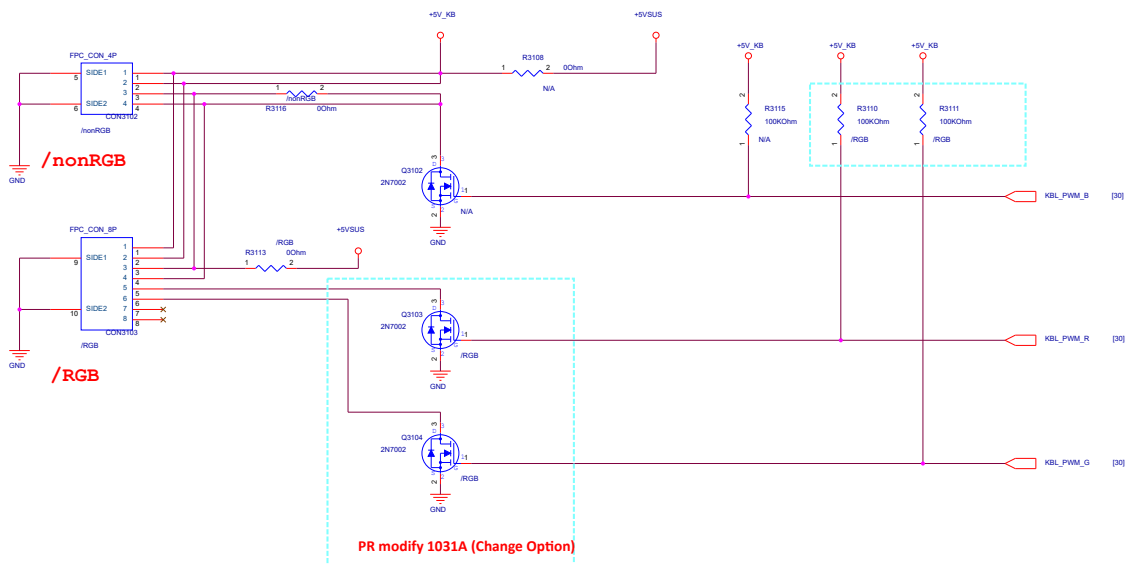
Title			
<Title>			
Size	Document Number		Rev
A	<Doc>		R1.0
Date:	Thursday, November 29, 2018	Sheet	19 of 103

Click pad

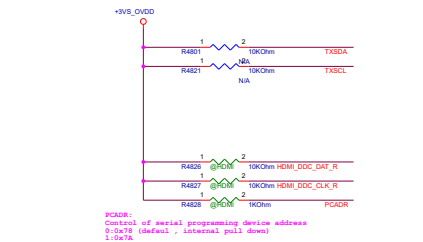
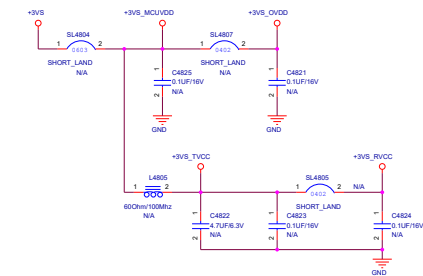
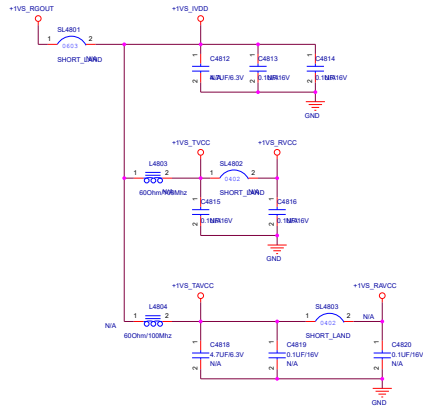
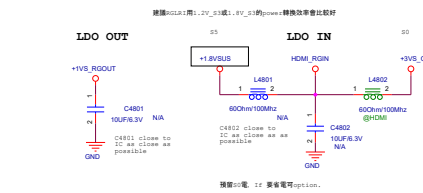
Slave (touchpad) address: 0X15



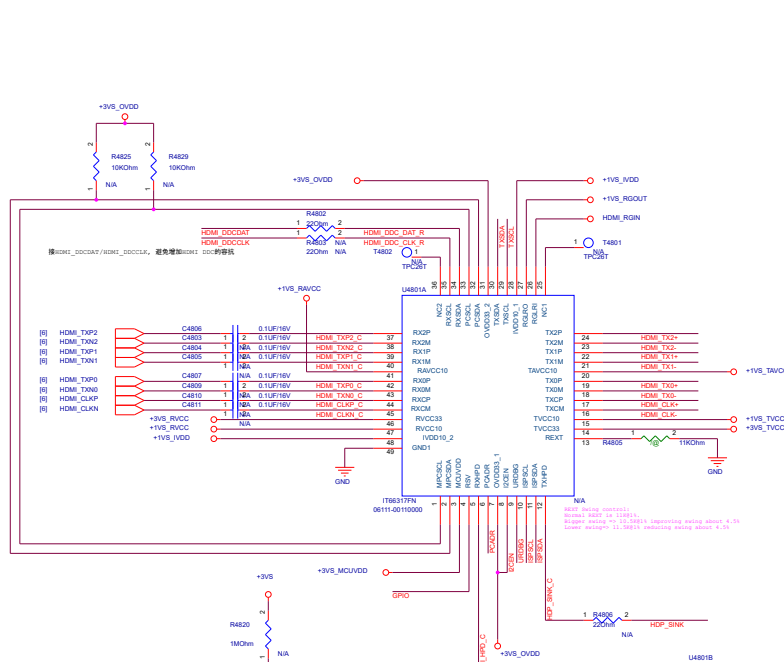
KB Backlight



Internal Regulator option



Retimer

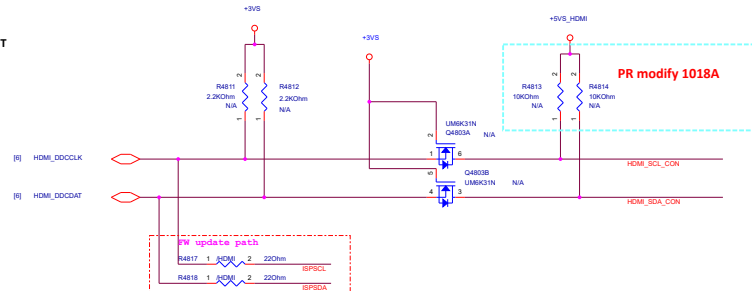


HW strapping

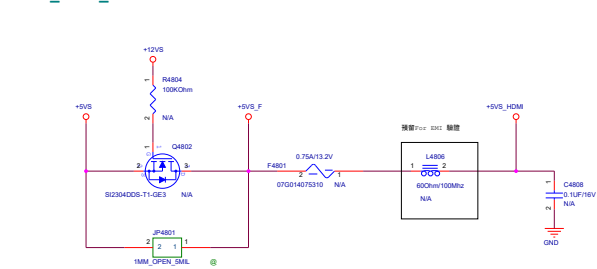
Output driving	0x20	0x2B0
Signal 1 (down)	0	0
Signal 2 (down)	0	1
Signal 3	1	0
Signal 4 (down)	1	1

Level 2 (default)

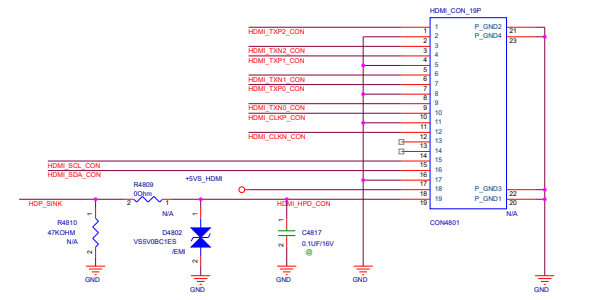
DDC LEVEL SHIFT



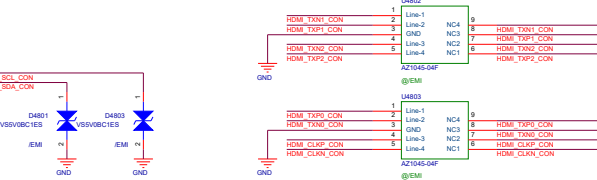
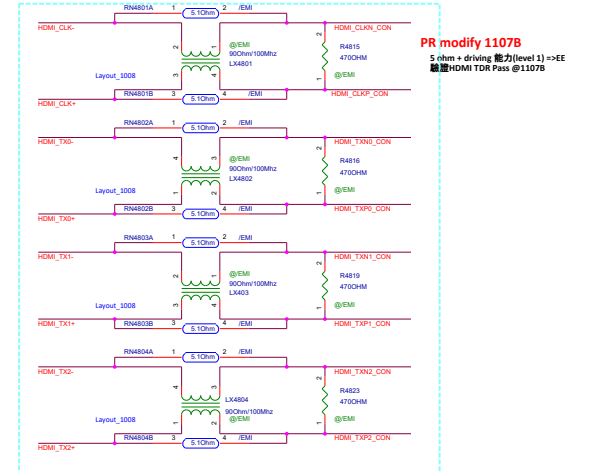
HDMI PWR +5V5_VDD



HDMI Conn.

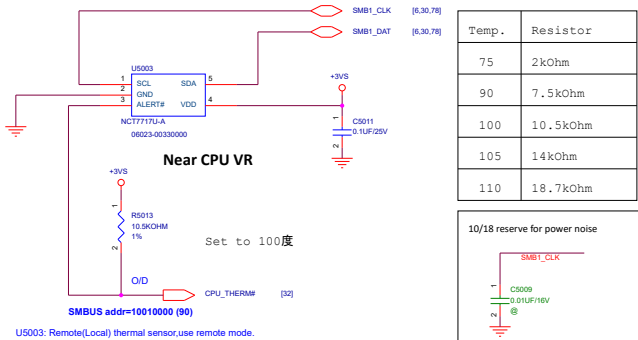


HDMI EMI



PR modify 1018A

CPU Thermal Sensor (CPU OTP使用, NCT7717)

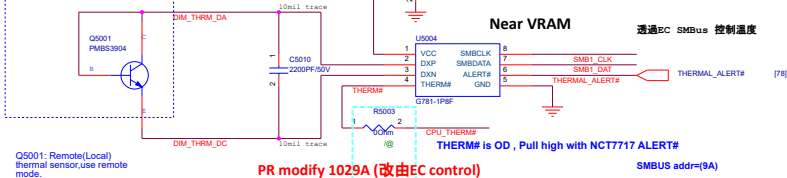


VRAM Thermal Sensor (為保護GPU VRAM使用(G781))

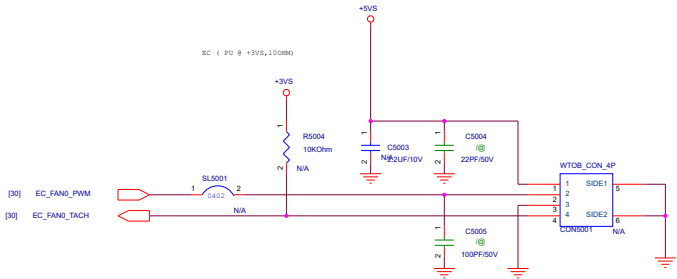
Near GPU VR

PHILIP PMBS3904

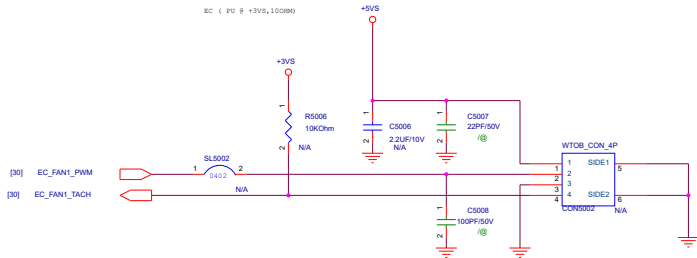
Place in the center of CPU socket.



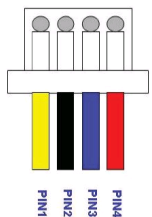
CPU FAN



GPU FAN



4Pins Fan Connector Pins Definition



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

--Variant Name--

SATA Conn. 2.5 HDD

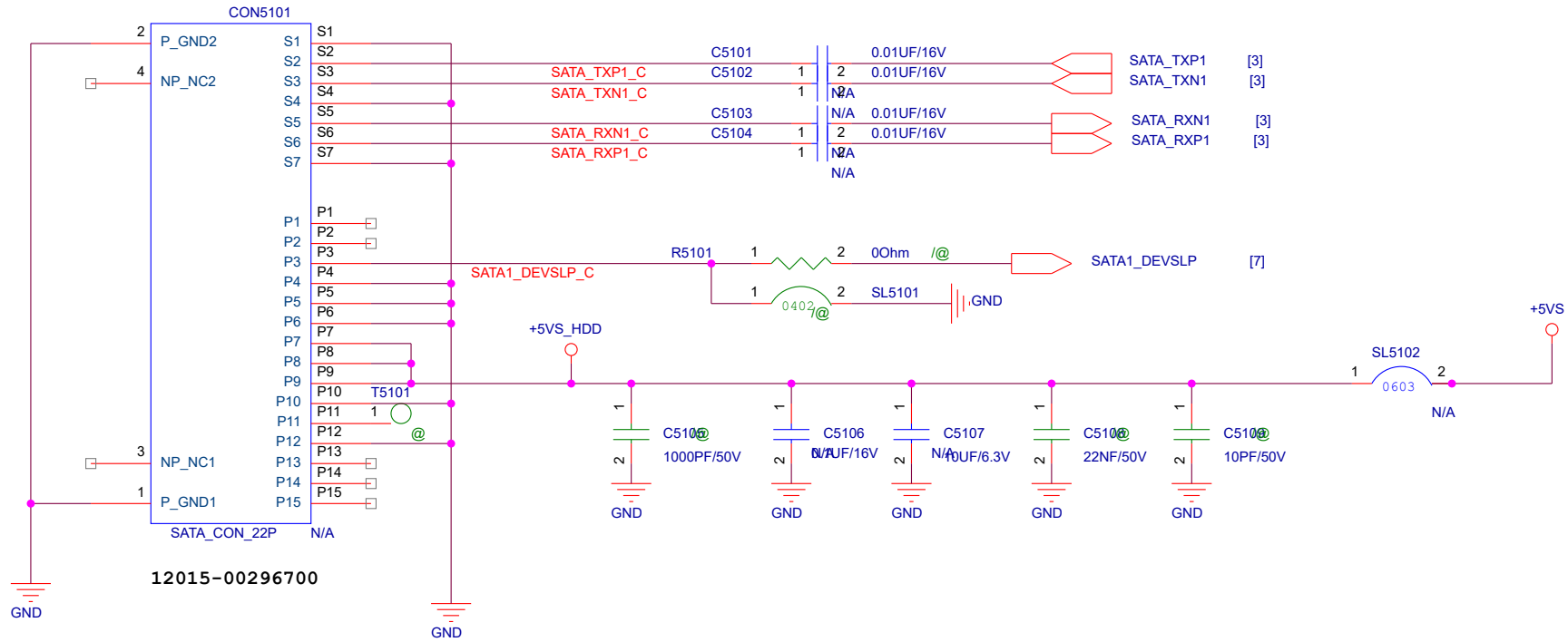
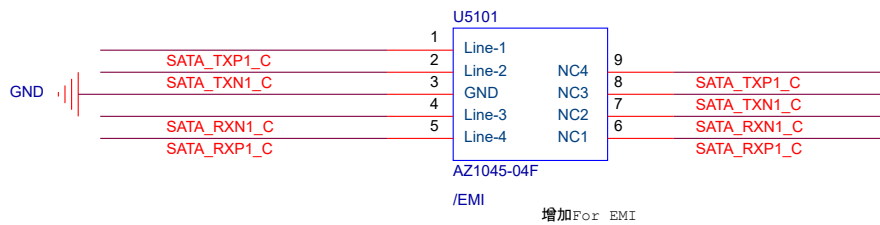



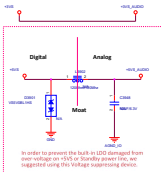
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

78	1	ENC	ENC	79
79	2	ENC	ENC	80
80	3	ENC	ENC	81
81	4	ENC	ENC	82
82	5	ENC	ENC	83
83	6	ENC	ENC	84
84	7	ENC	ENC	85
85	8	ENC	ENC	86
86	9	ENC	ENC	87
87	10	ENC	ENC	88
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89	12	ENC	ENC	90
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91	14	ENC	ENC	92
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93	16	ENC	ENC	94
94	17	ENC	ENC	95
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97	20	ENC	ENC	98
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163	86	ENC	ENC	164
164	87	ENC	ENC	165
165	88	ENC	ENC	166
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262	185	ENC	ENC	263
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359	282	ENC	ENC	360
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361	284	ENC	ENC	362
362	285	ENC	ENC	363
363	286	ENC	ENC	364
364	287	ENC	ENC	365
365	288	ENC	ENC	366
366	289	ENC	ENC	367
367	290	ENC	ENC	368
368	291	ENC	ENC	369
369	292	ENC	ENC	370
370	293	ENC	ENC	371
371	294	ENC	ENC	372
372	295	ENC	ENC	373
373	296	ENC	ENC	374
374	297	ENC	ENC	375
375	298	ENC	ENC	376
376	299	ENC	ENC	377
377	300	ENC	ENC	378
378	301	ENC	ENC	379
379	302	ENC	ENC	380
380	303	ENC	ENC	381
381	304	ENC	ENC	382
382	305	ENC	ENC	383
383	306	ENC	ENC	384
384	307	ENC	ENC	385
385	308	ENC	ENC	386
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387	310	ENC	ENC	388
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389	312	ENC	ENC	390
390	313	ENC	ENC	391
391	3			

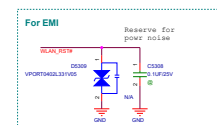
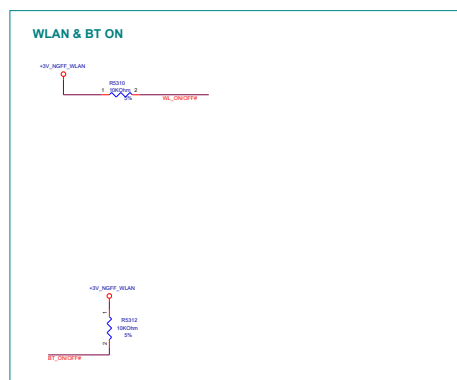
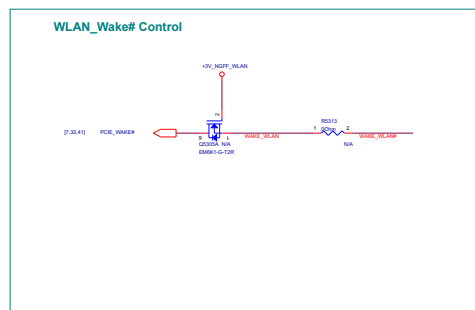
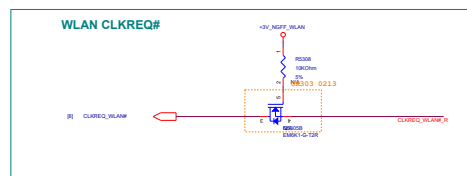
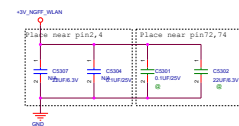
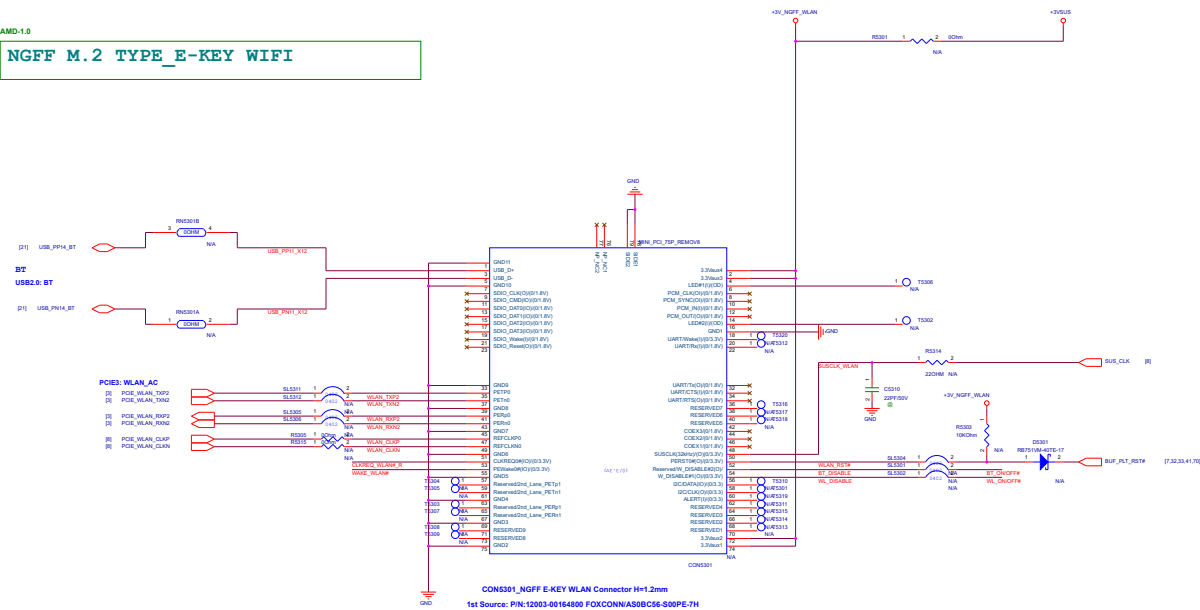


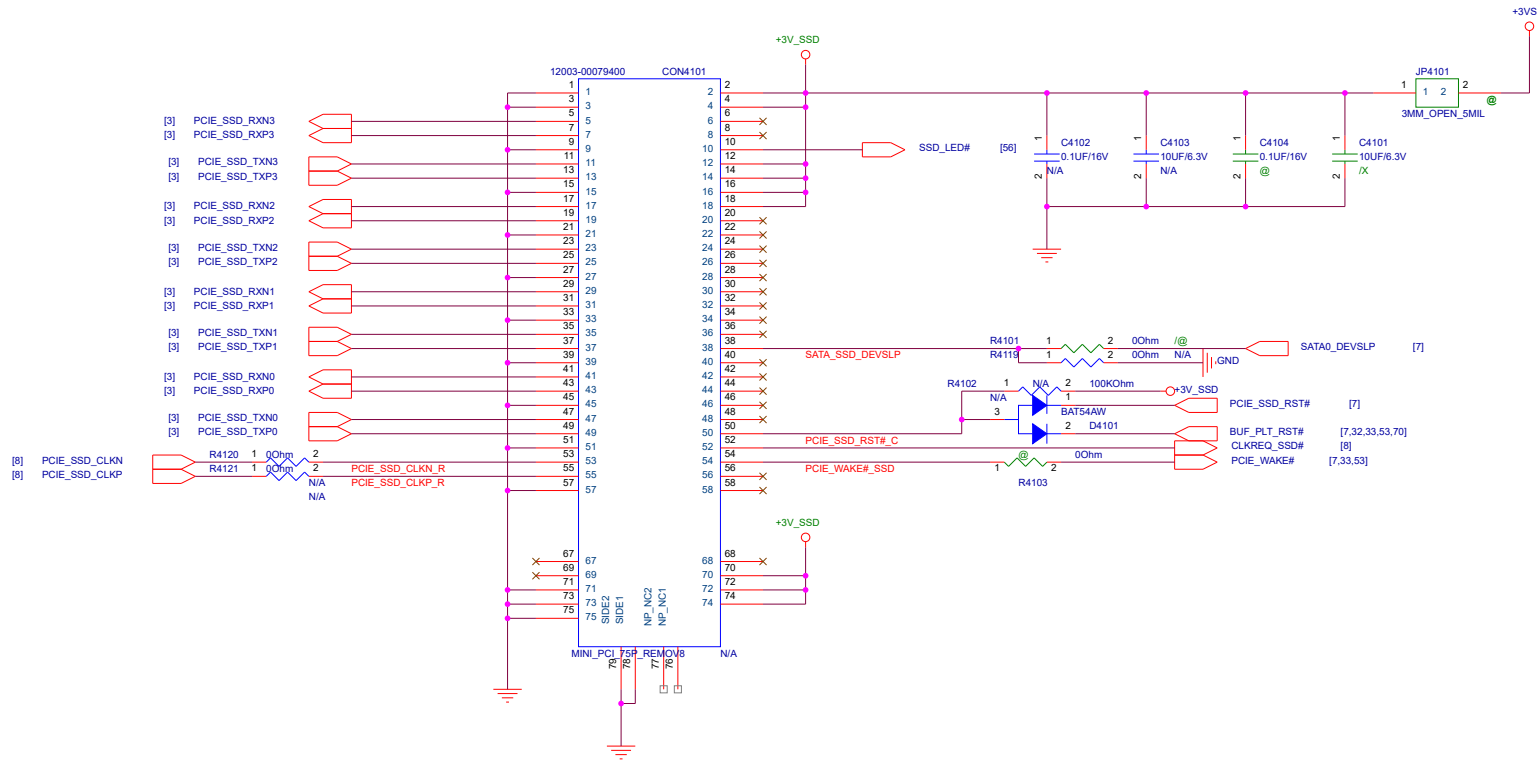
<Variant Name>

		Title : SATA_HDD	
ASUSTeK COMPUTER INC. NB3		Engineer: EE3	
Size A	Project Name FX505DY		Rev R1.0
Date: Thursday, November 29, 2018		Sheet 51 of 103	

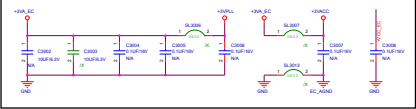


NGFF M.2 TYPE E-KEY WIFI

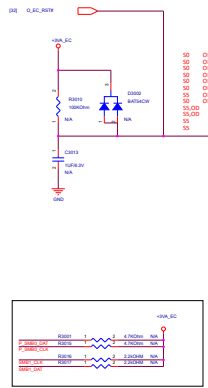




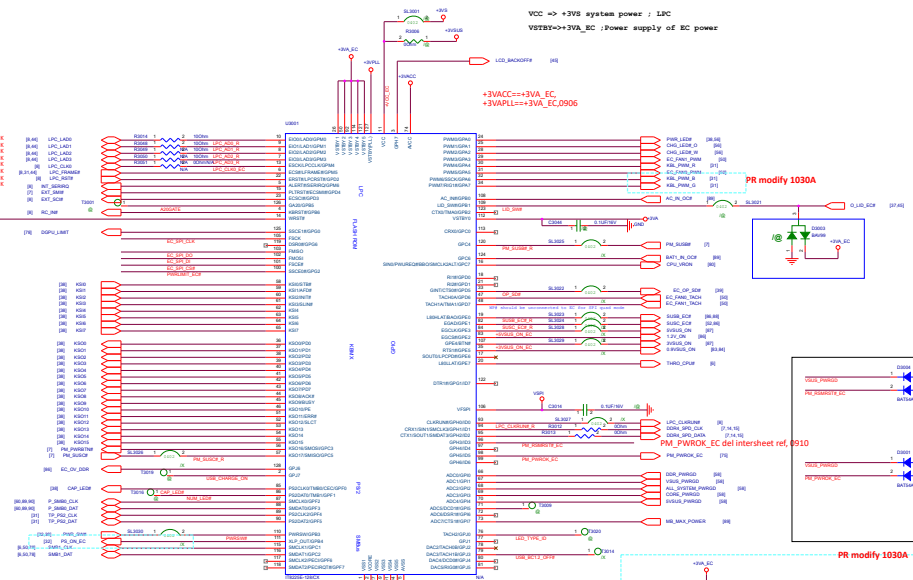
EC Power



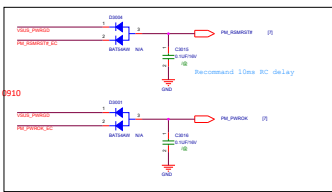
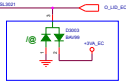
PR modify 1018A

[illegible]

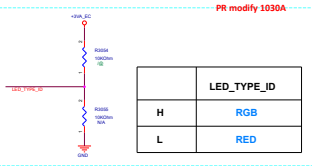
Modify 1031A_Change PS_ON to PS_ON_EC



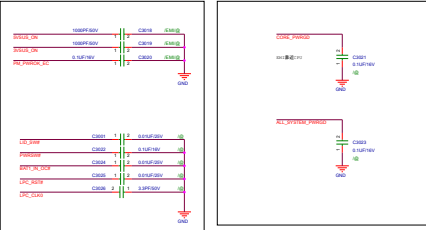
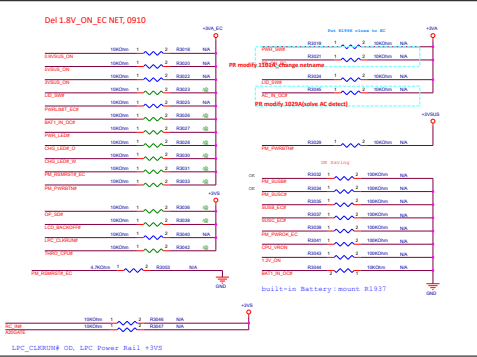
PR modify 1030A



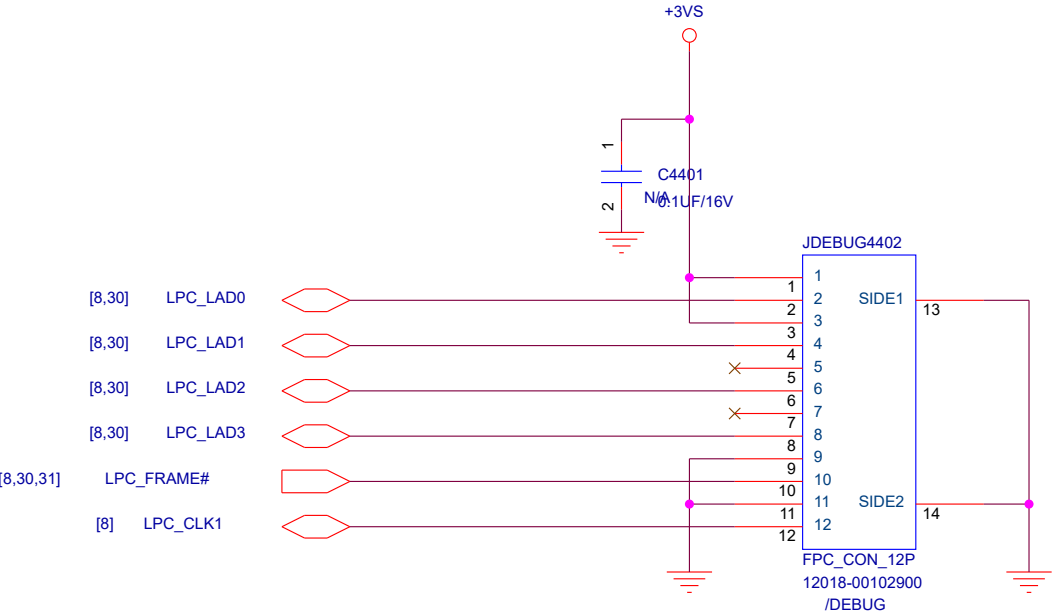
PR modify 1030A



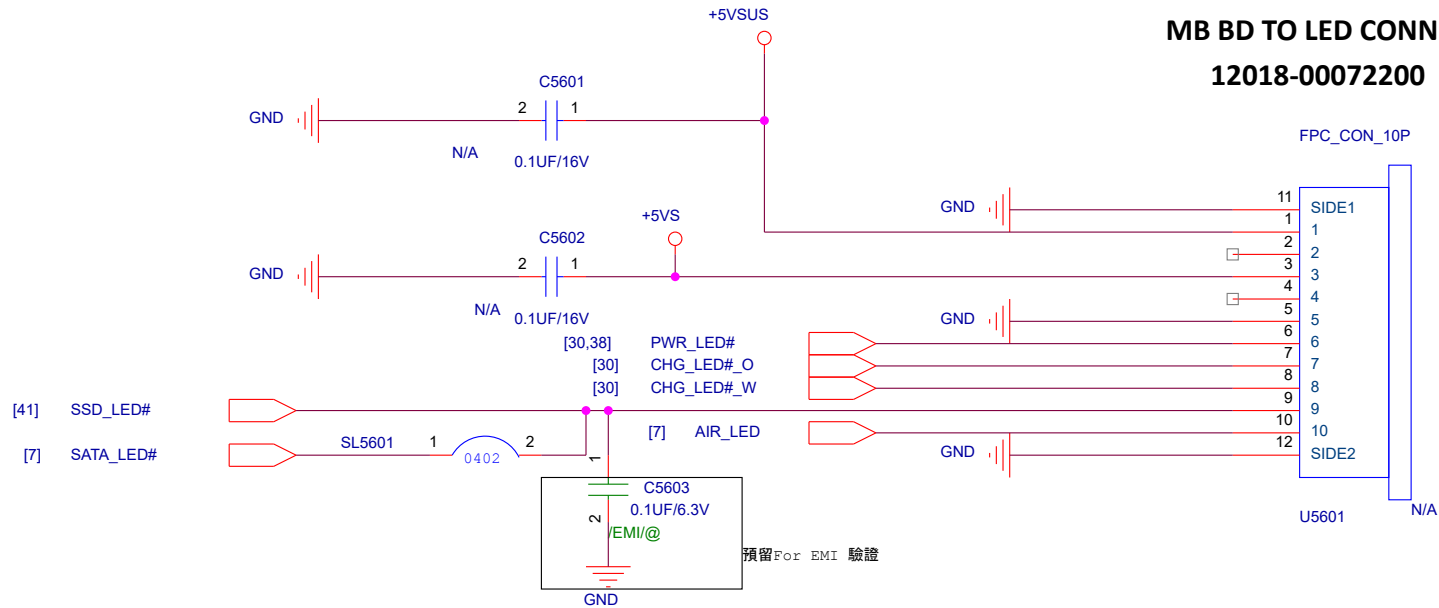
	LED_TYPE_ID
H	RGB
L	RED



LPC Debug Port



MB BD TO LED CONN 12018-00072200



Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION

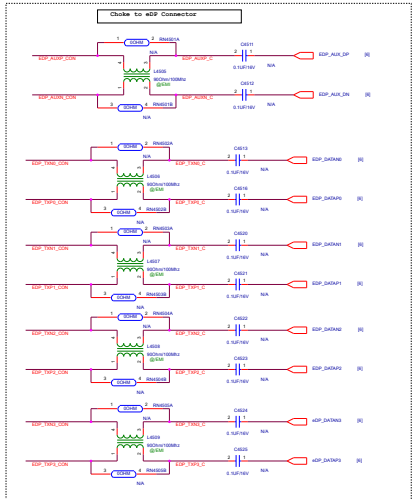
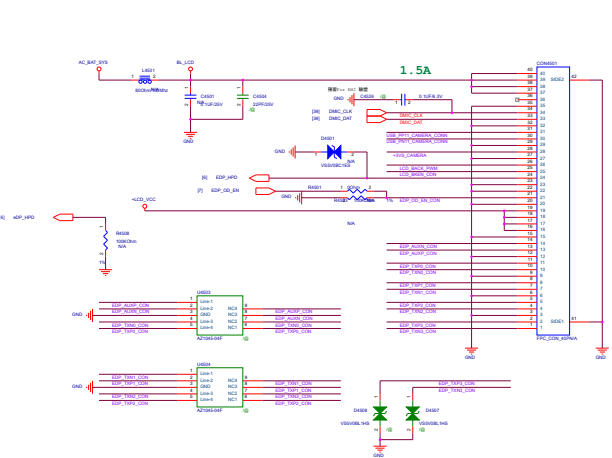


HDD LED

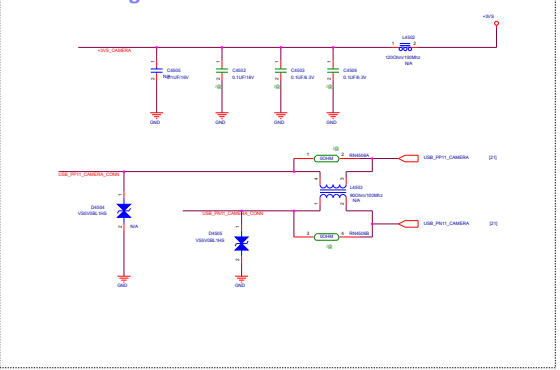
JS	Project Name	Rev
	FX505DY	R1.0
_Side_LED		

Size A	Dept.: ASUSTek COMPUTER INC. Engineer: RD2 EE3		
Date: Thursday, November 29, 2018	Sheet	56	of 103

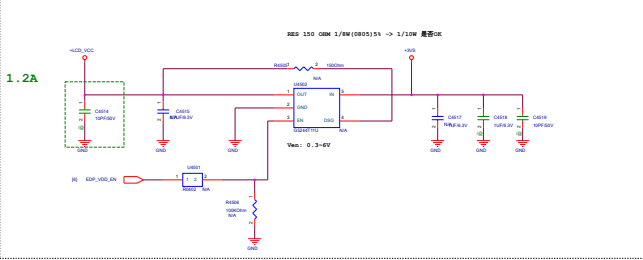
eDP Connector (LVDS)



Camera Signal



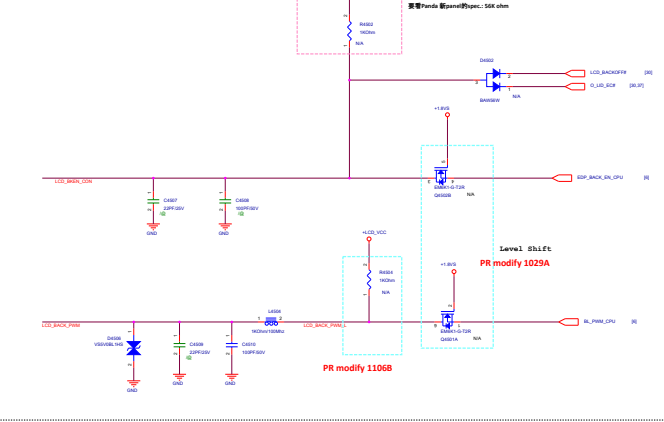
LCD VDDEN / +LED_VCC



Pin Description

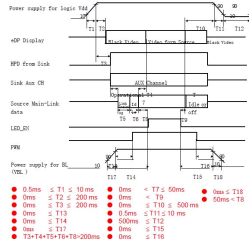
PIN	NAME	PIN FUNCTION
1	OUT	Switch Output: Output MOSFET Source. Typically connect to switched side of load.
2	GND	Ground
3	EN	Enable: Logic level enable input. Make sure EN pin never floating.
4	DSG	Shutdown Discharge: Open-drain N-MOS. It will turned on when G5244 is turned off. By connecting a resistor from DSG to OUT pin, user can discharge OUT when G5244 is shutdown.
5.	IN	Input Supply: Output MOSFET Drain, which also supplies IC's internal circuitry. Connect to positive supply.

Control Signal (LCD/BL)



1. POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

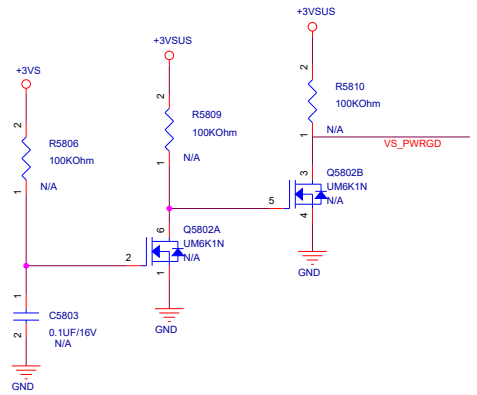
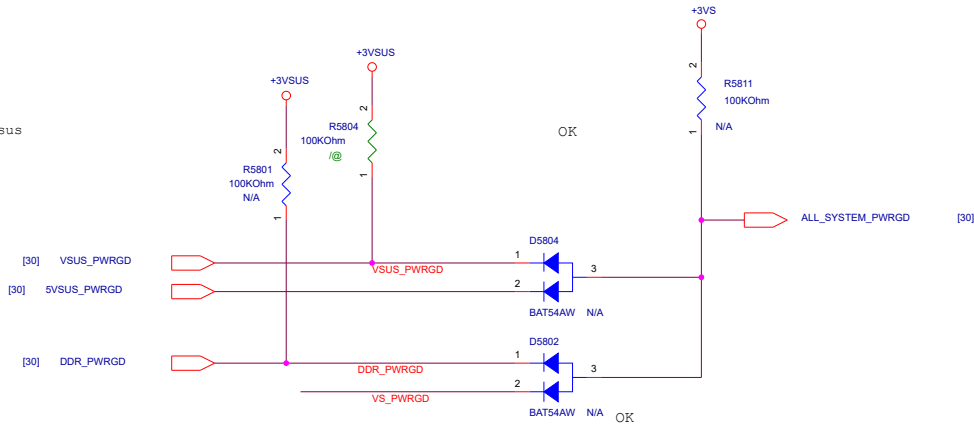


- Notes:
- 1. When the power supply VDDEN is 0V, keep the level of input signals on the low or high impedance.
- 2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal was valid.

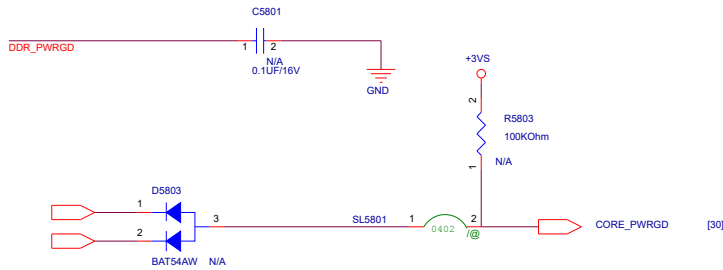
POWER GOOD DETECTOR

0.95/1.8/3/5vsus

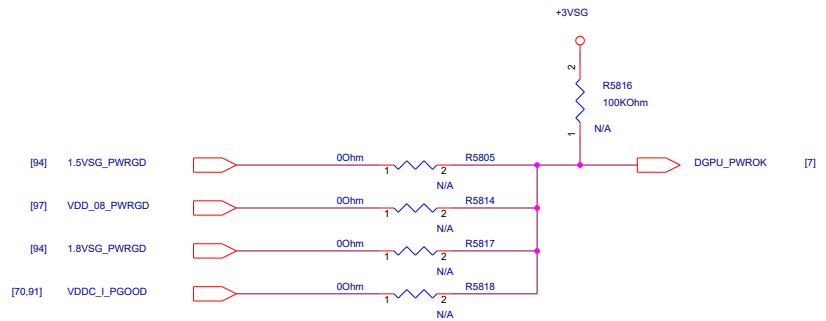
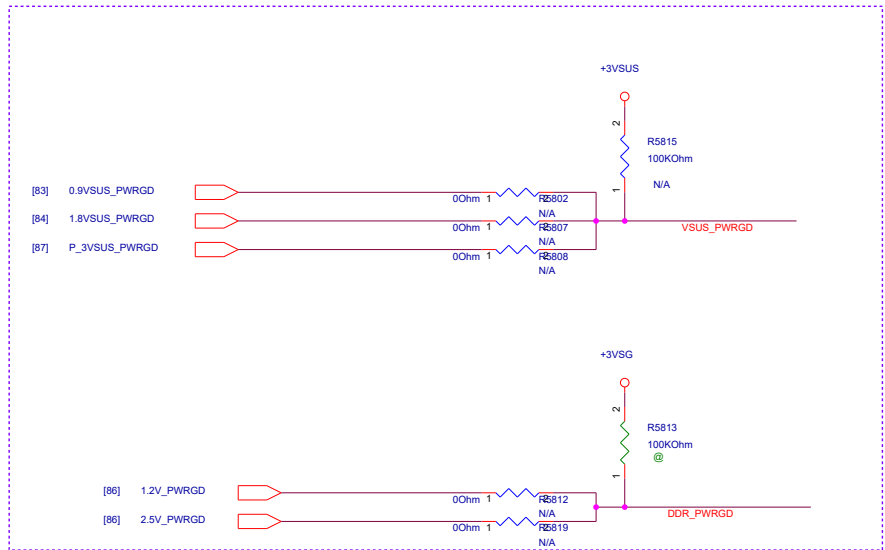
DEEP S3



Power Good

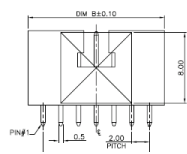


Power Good

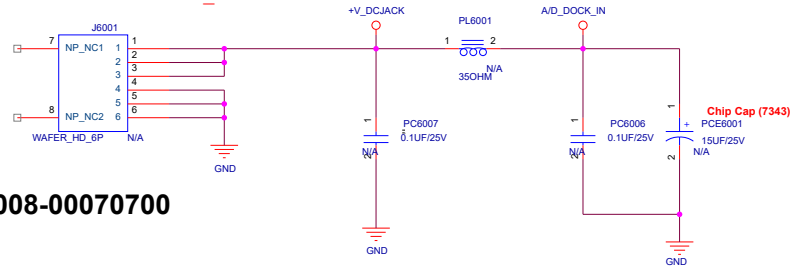


DC-IN Connector

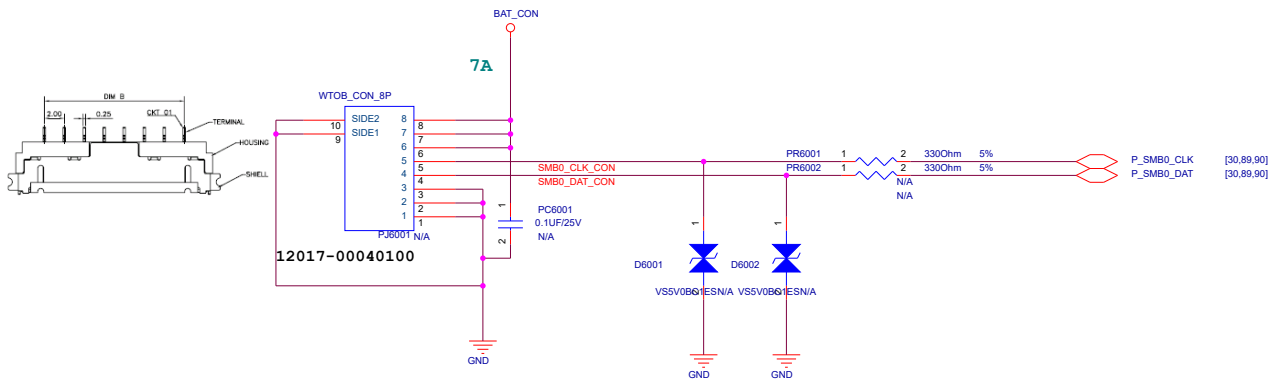
For new 6 Phi 4 Pin DC_Jack



12008-00070700

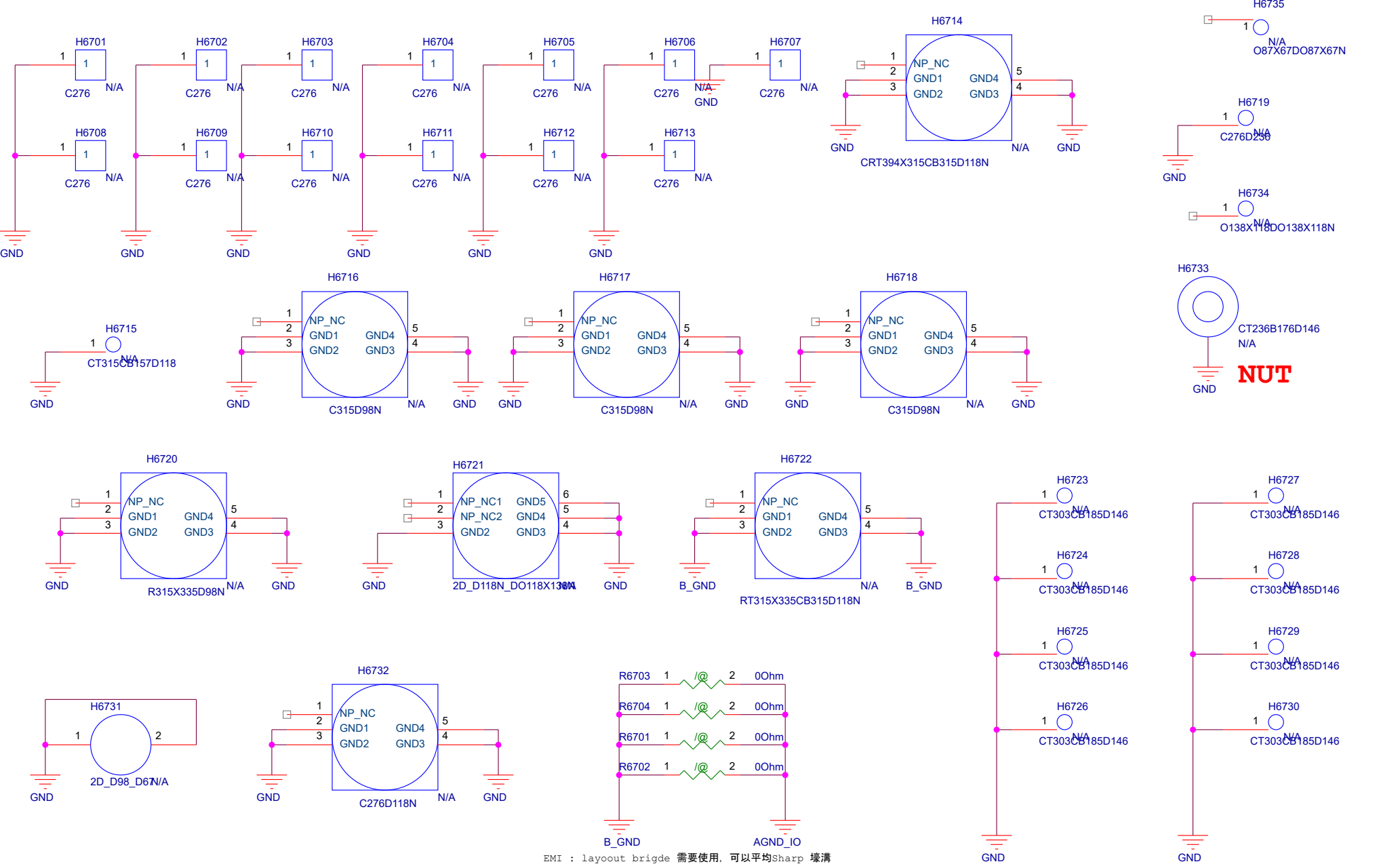


Battery Connector




Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS		Project Name	Rev
		FX505DY	R1.0
Title : DC & BAT IN			
Size	Dept.:	Engineer:	
A3	NB_Power team	CS Lin	
Date:	Thursday, November 29, 2018	Sheet	60 of 103

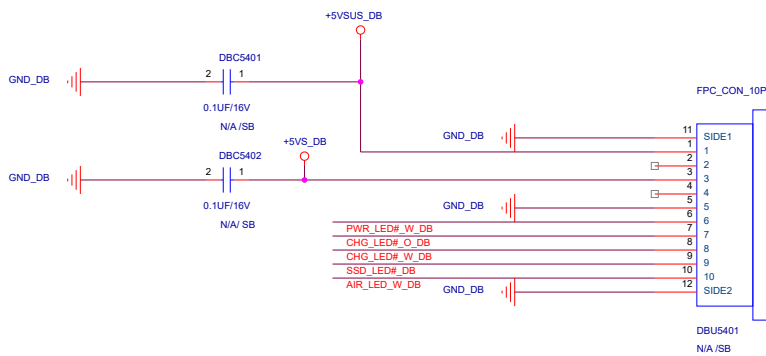


<Variant Name>

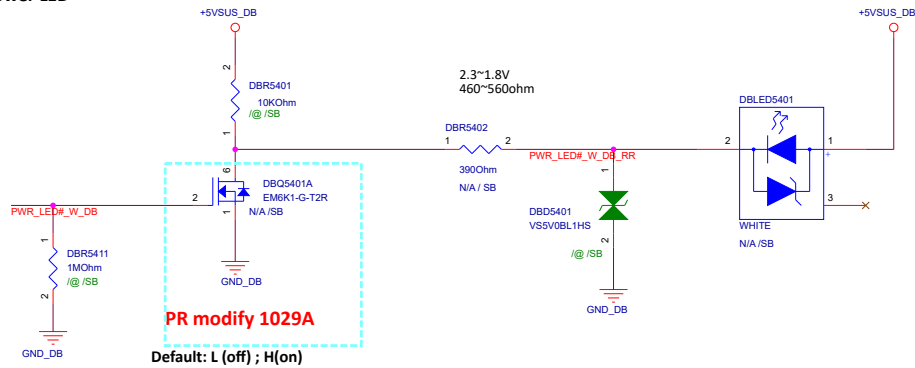
		Title : SREW HOLE	
ASUSTeK COMPUTER INC. NB4		Engineer: EE	
Size A	Project Name FX505DY		Rev R1.0

		Project Name	Rev
		FX505DY	R1.0
Title : AMD_CPU_GND			
Size B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3		
Date: Thursday, November 29, 2018	Sheet	68	of 103

SB_Side LED

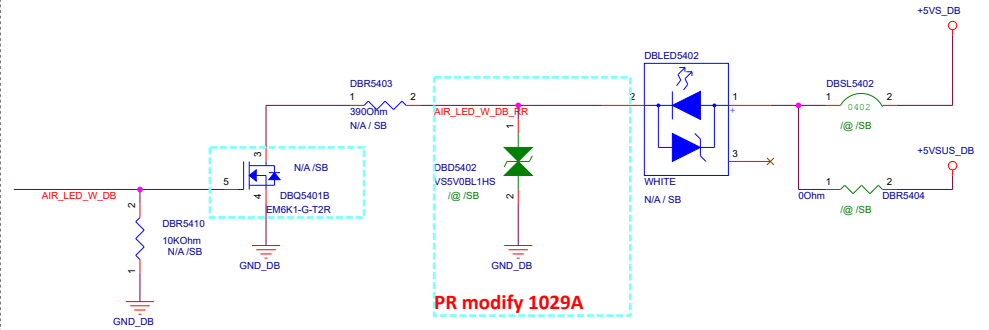


Power LED

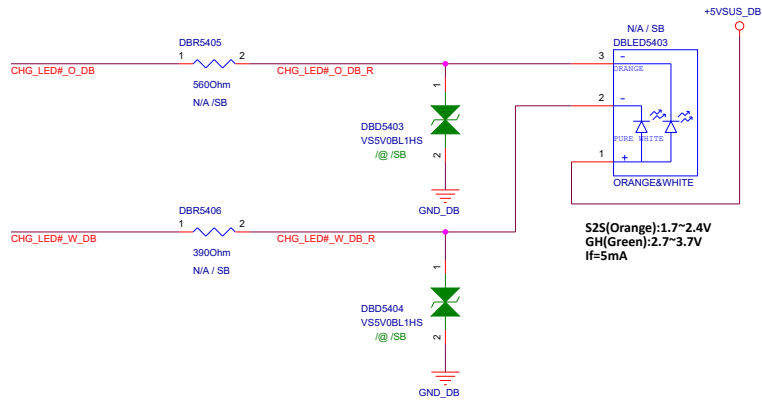


AIR PLANE LED(White)

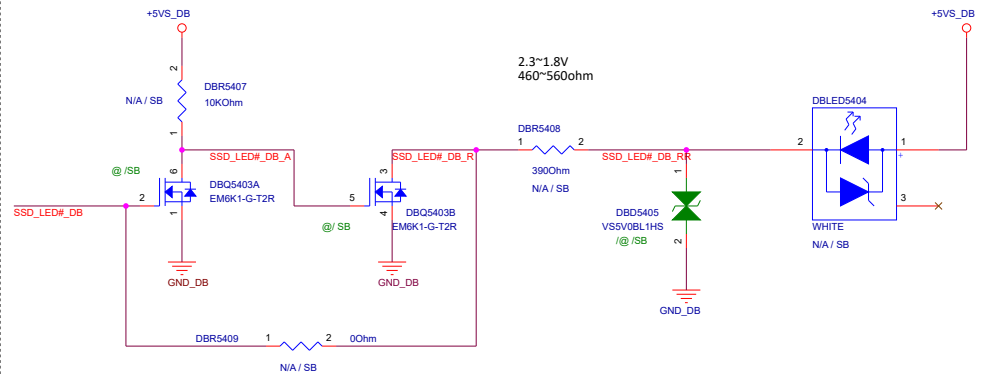
NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF



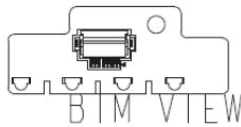
Charger LED(White/Orange)



HDD LED

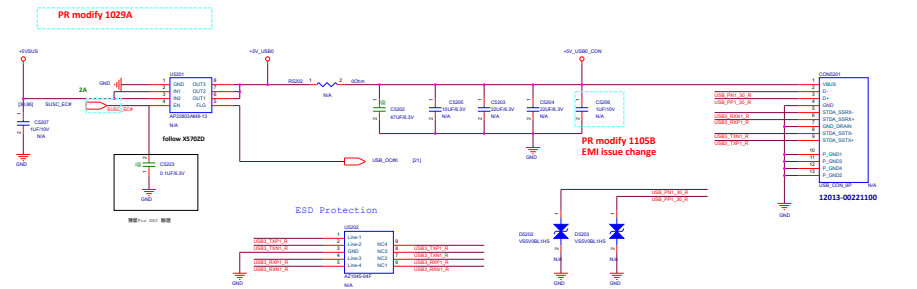
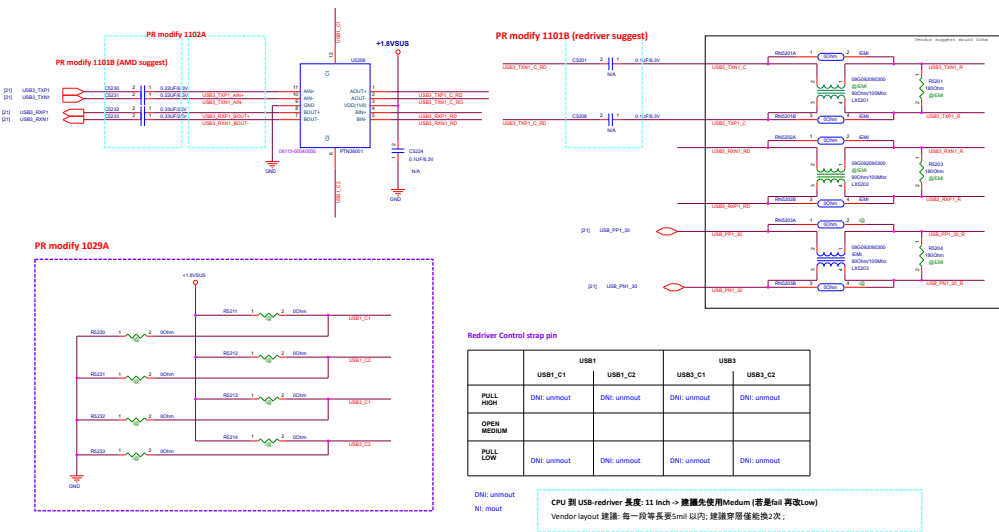


PCB/ID LOCATION

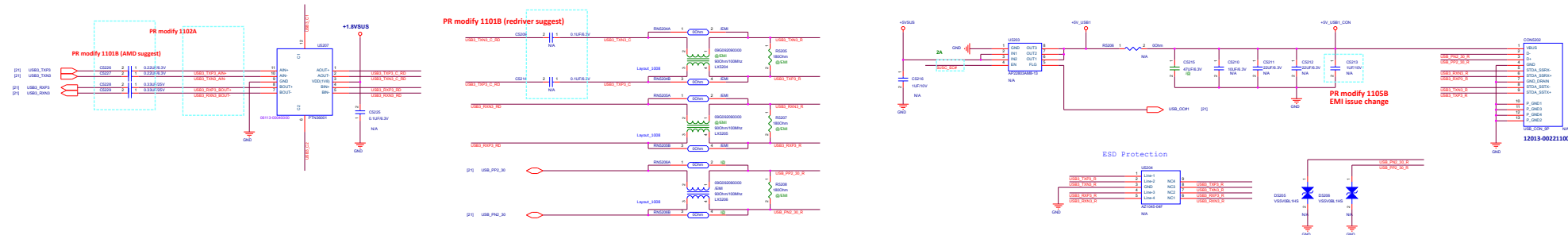


Tooling Hole

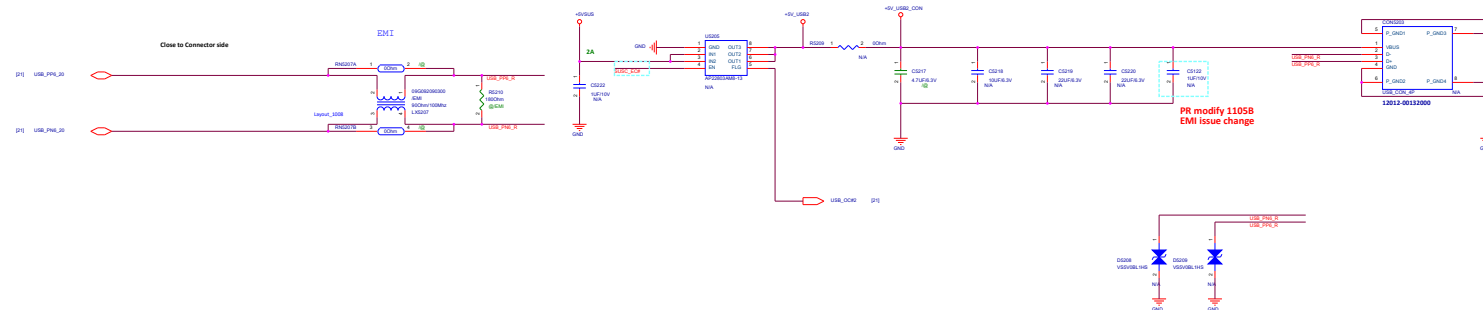


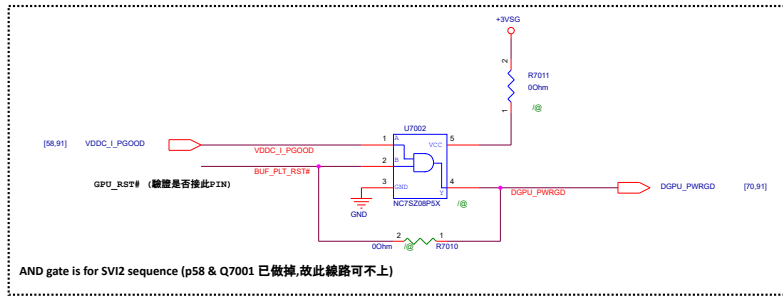
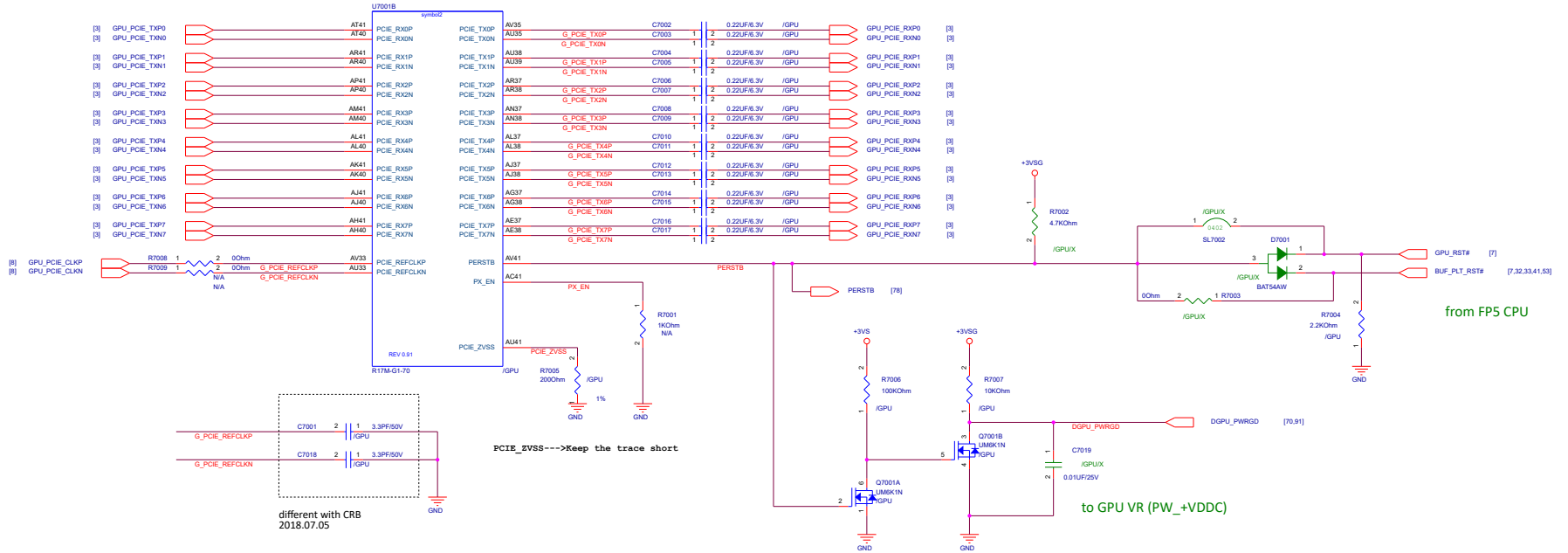


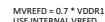
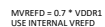
USB3.0_Port 3

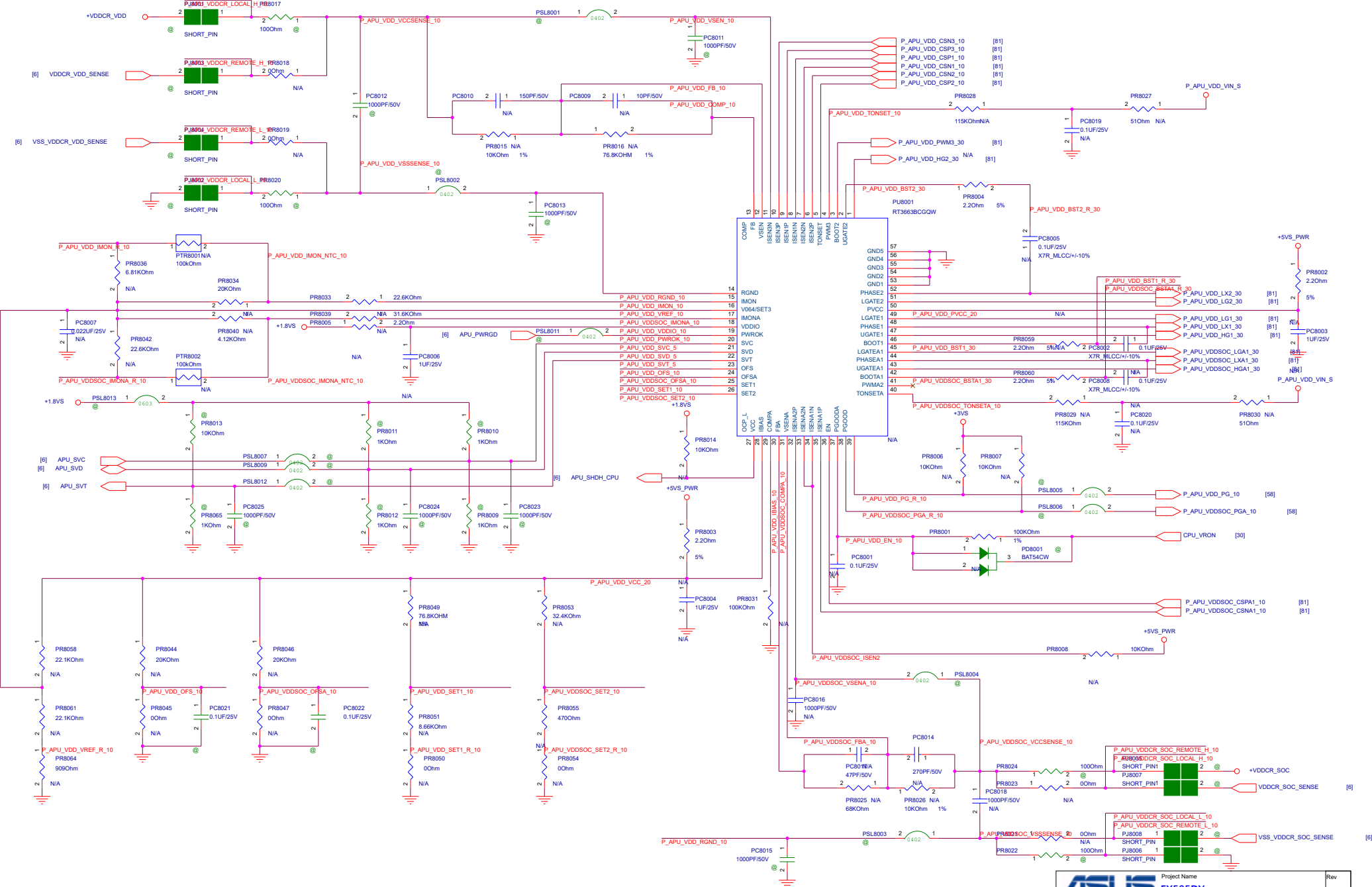


USB2.0_Port 0



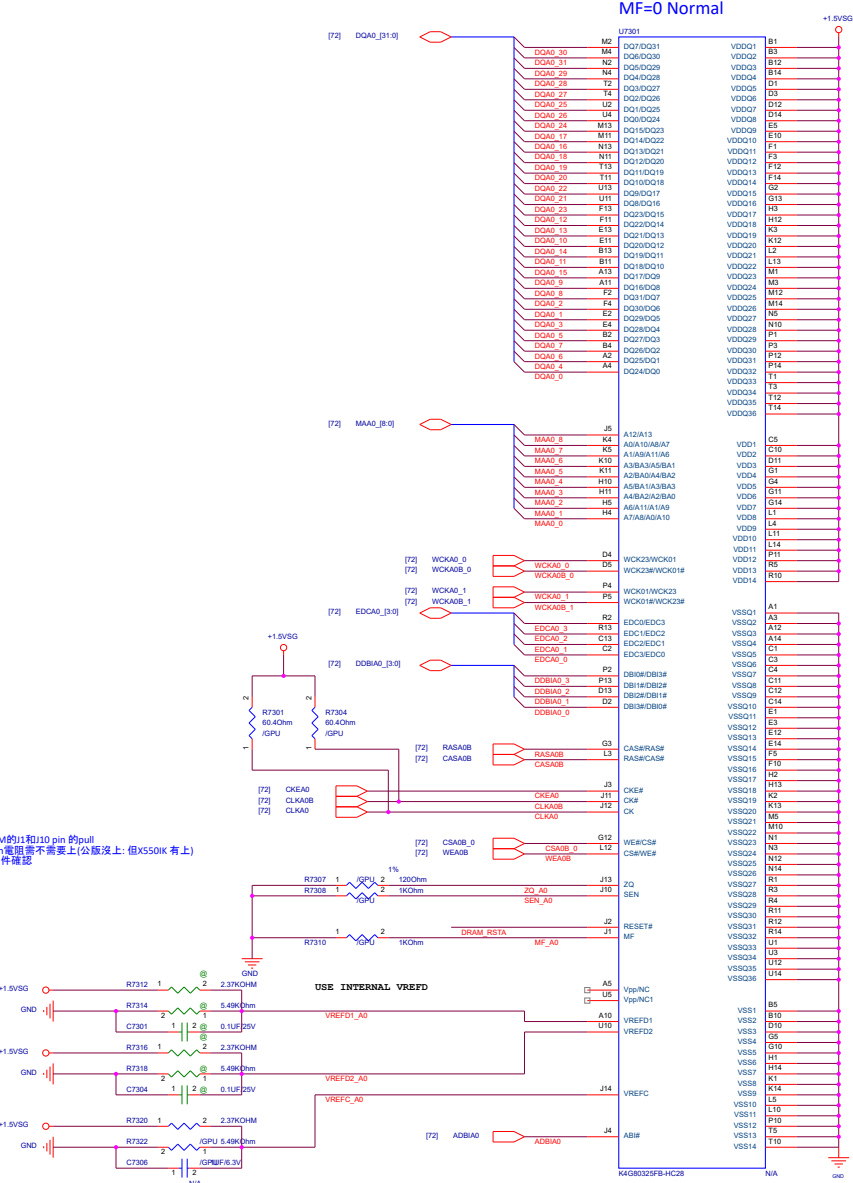




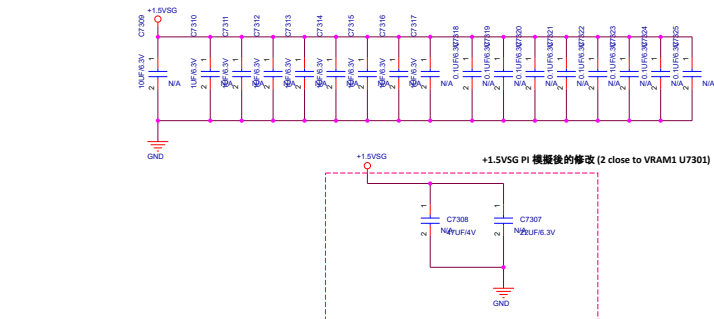


FBA Partition Memory (1 of 2)

MF=0 Normal



VDDQ/VDD (Memory Parts) 1pcs 10uF; 8pcs 1uF; 10pcs 1uF

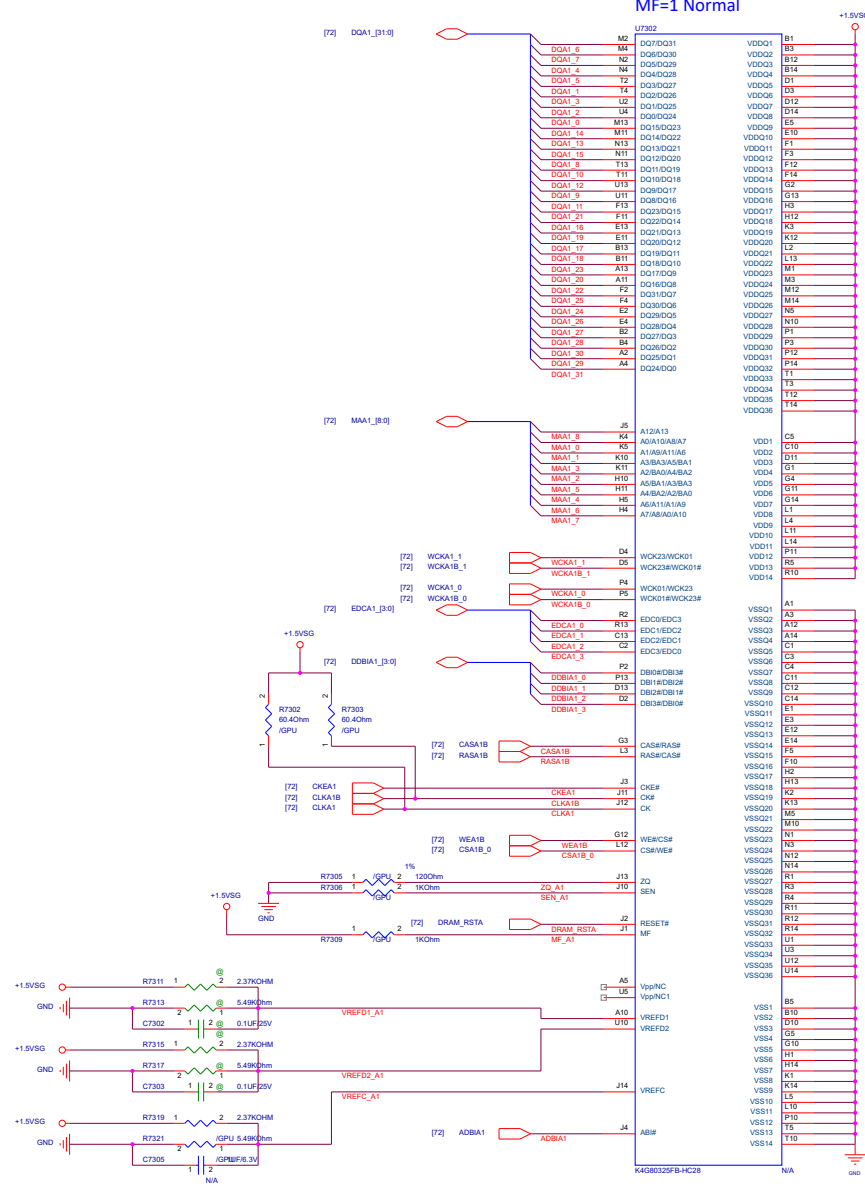


GDDR5 256x32_7.0G (8Gb)

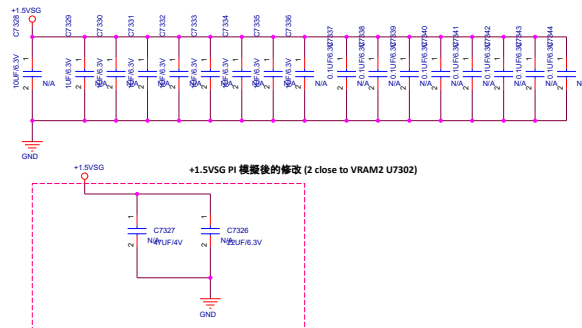
Priority	Company	Model Name	Base	Voltage	Speed	MP Schedule	ASUS P/N
1	Samsung	K4G80325FB-HC28	Samsung	256x32	1.35V/1.55V	6.0G/7.0G	03008-00050000
2	Micron	MT151256M32HF-70:A	Micron	256x32	1.35V/1.5V	6.0G/7.0G	03008-00050400

FBA Partition Memory (2 of 2)

MF=1 Normal



VDDQ/VDD (Memory Parts) 1pcs 10uF; 8pcs 1uF; 10pcs 1uF



ASUS X550TU

Title : DGPU_GDDR5_1

Size : Custom

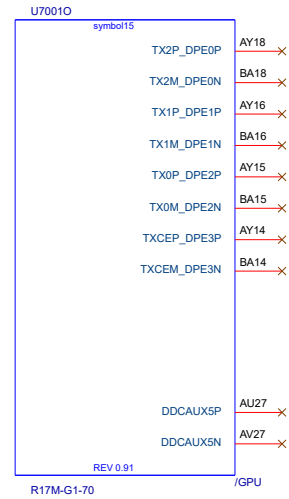
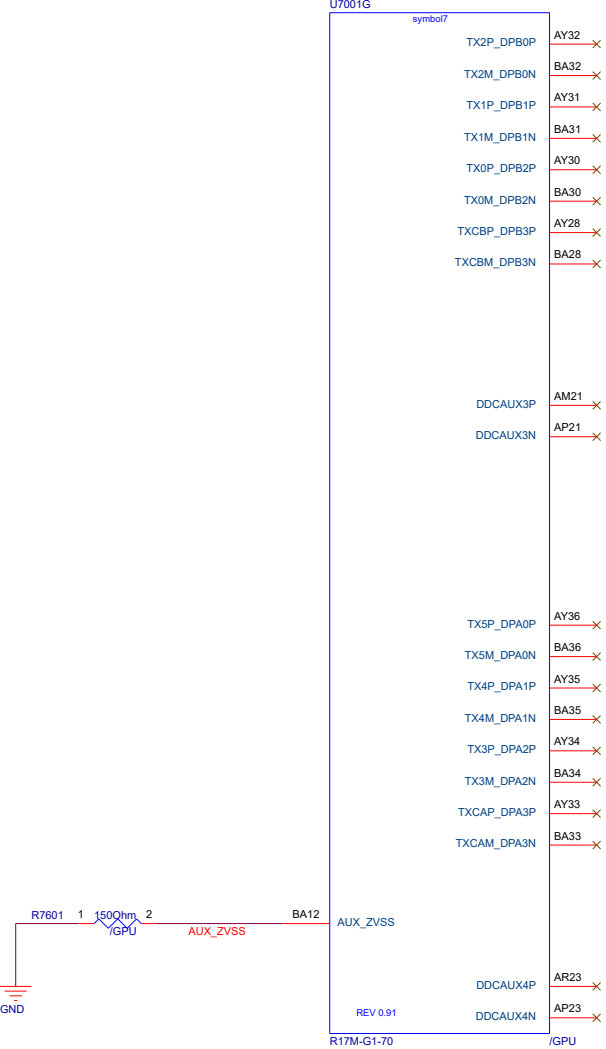
Date: Thursday, November 25, 2016

Sheet 73 of 103

Rev R1.0

Dept.: ASUSTek Computer Inc.

Engineer: RD1/EE2

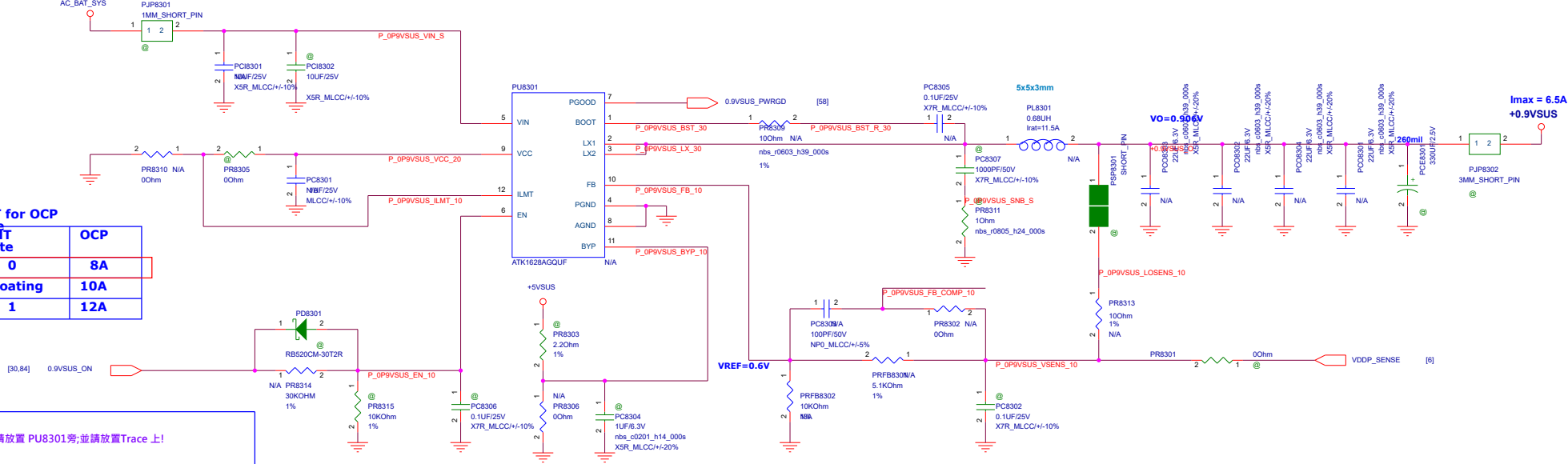


ILMT for OCP

ILMT State	OCP
0	8A
Floating	10A
1	12A

PT830* 請放置 PU8301旁;並請放置Trace 上!

P_OP9VSUS_LX_30



<Variant Name>


ASUS	Project Name FX505DY	Rev R1.0
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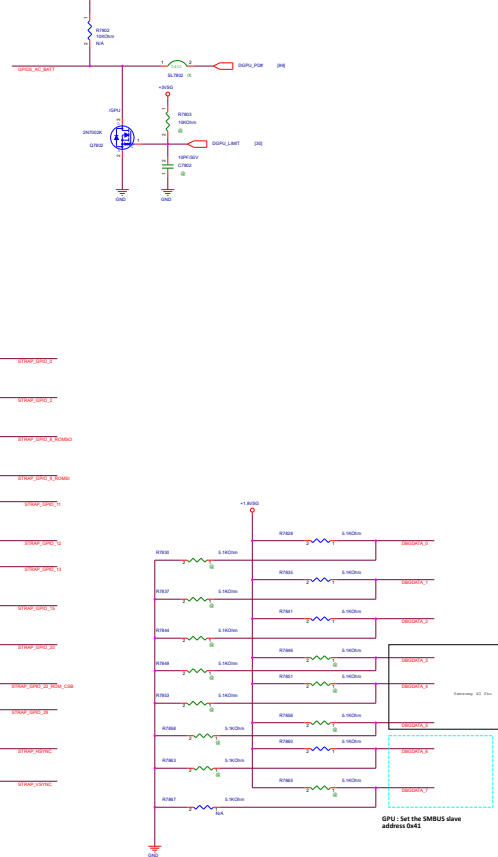
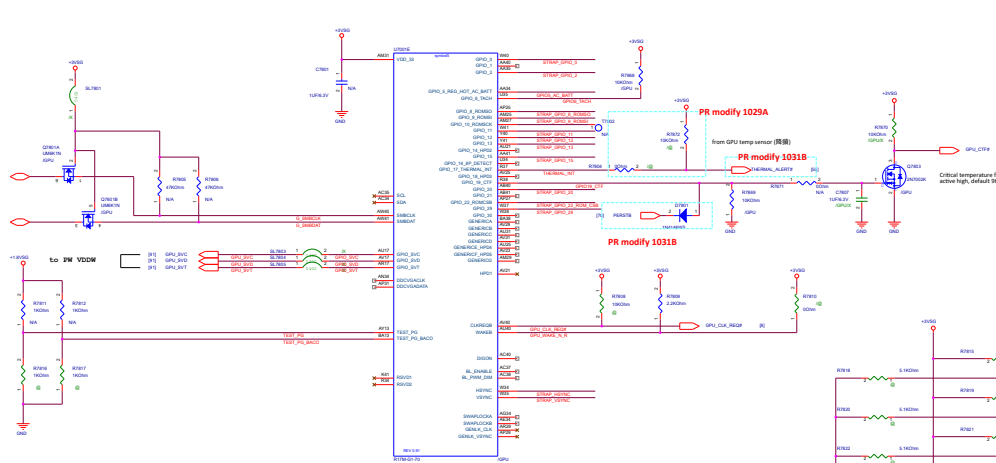
Title :	PW_+0.9VSUS
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Size A3	Dept.: NB Power team	Engineer: CS Lin
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Date: Thursday, November 29, 2018	Sheet 83 of 103
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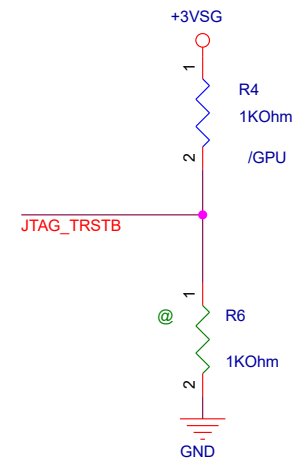
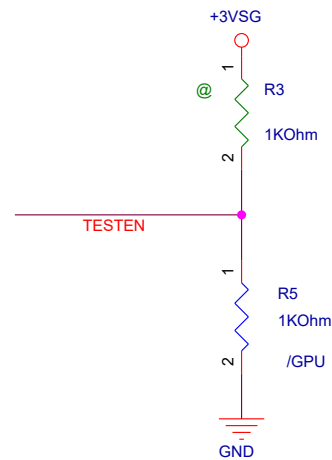
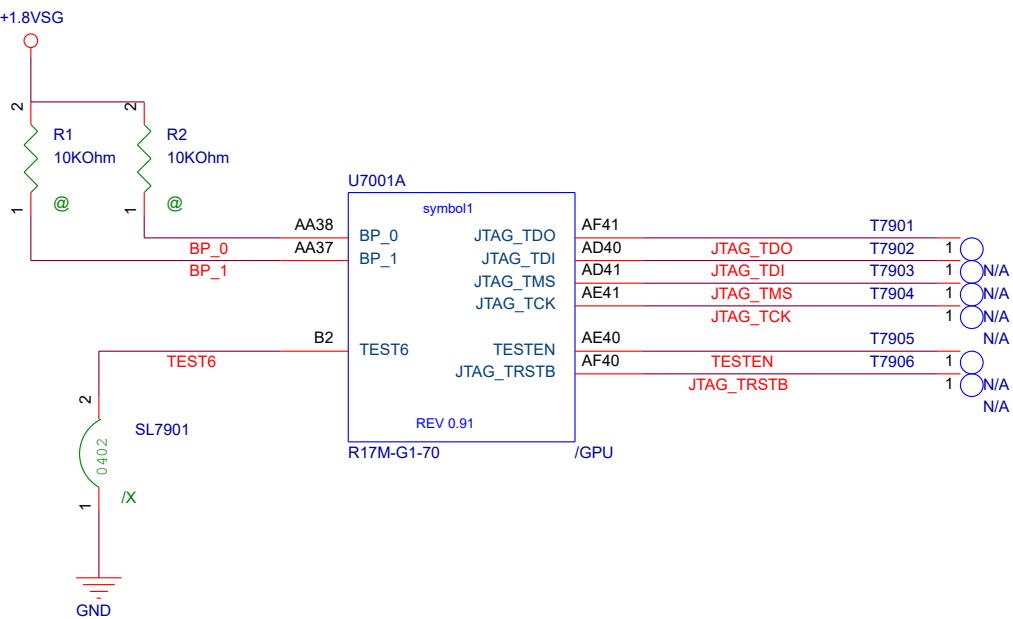
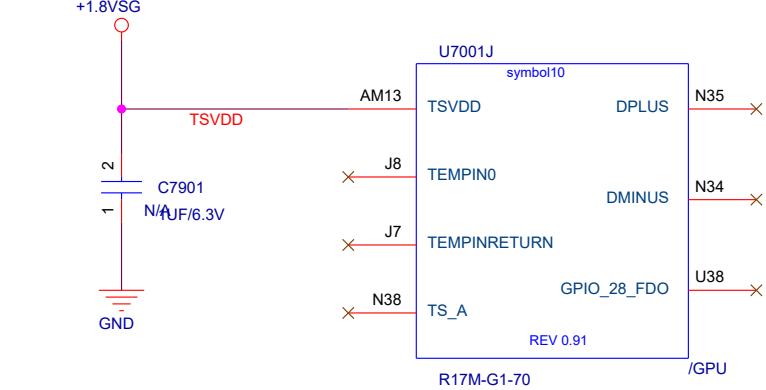
TX2P_DPD0P	AY22	✗
TX2M_DPD0N	BA22	✗
TX1P_DPD1P	AY21	✗
TX1M_DPD1N	BA21	✗
TX0P_DPD2P	AY20	✗
TX0M_DPD2N	BA20	✗
TXCDP_DPD3P	AY19	✗
TXCDM_DPD3N	BA19	✗
AUX1P	AY11	✗
AUX1N	BA11	✗
DDC1CLK	AY10	✗
DDC1DATA	BA10	✗
TX5P_DPC0P	AY27	✗
TX5M_DPC0N	BA27	✗
TX4P_DPC1P	AY26	✗
TX4M_DPC1N	BA26	✗
TX3P_DPC2P	AY25	✗
TX3M_DPC2N	BA25	✗
TXCCP_DPC3P	AY24	✗
TXCCM_DPC3N	BA24	✗
AUX2P	AP19	✗
AUX2N	AM19	✗
DDC2CLK	AV19	✗
DDC2DATA	AU19	✗

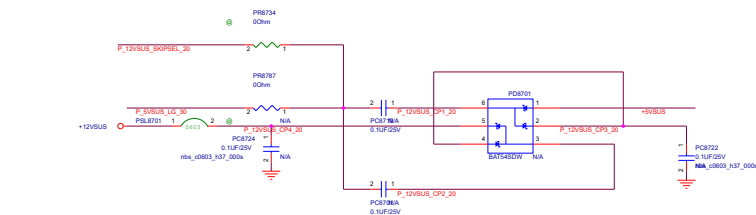
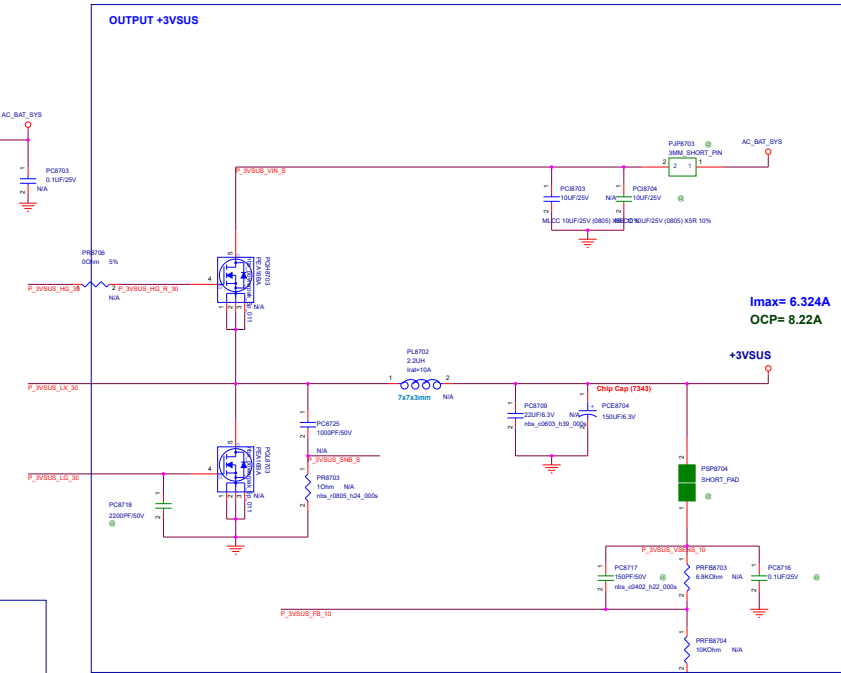
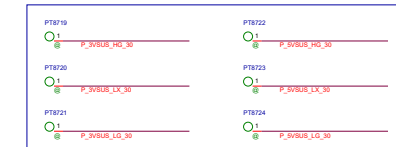
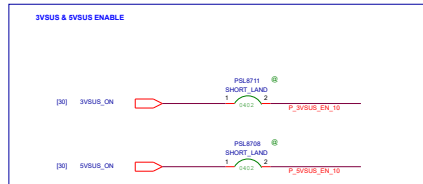
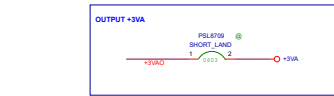
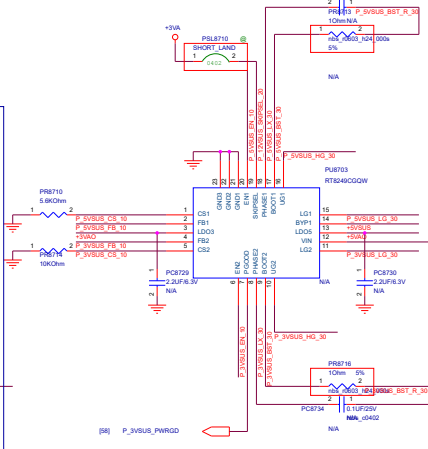
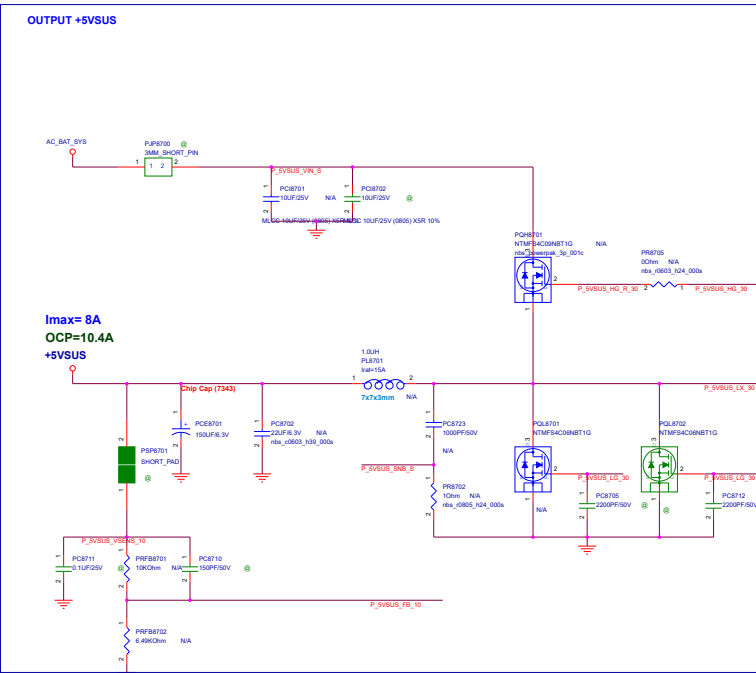
		Project Name		Rev
		X550IU		R1.0
Title : DGPU_TMDP				
Size	Dept.: ASUSTek Computer Inc.		Engineer:	RD1/EE2
Date: Thursday, November 29, 2018		Sheet	77	of 103

[illegible][illegible]

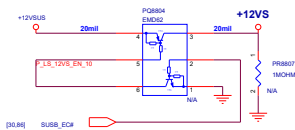
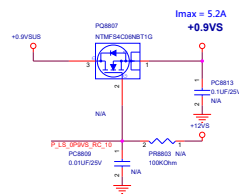
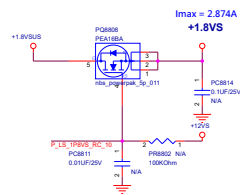
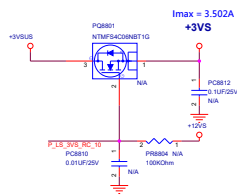
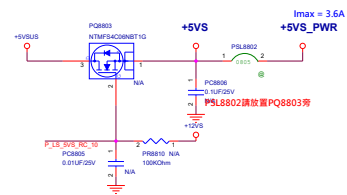
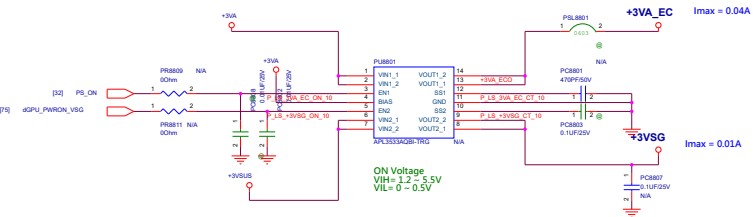
SR SKU Table
000=SAMSUNG 4G 03008-00050500 -----50W BOM
001=MICRON 4G 03008-00050400 -----60W BOM

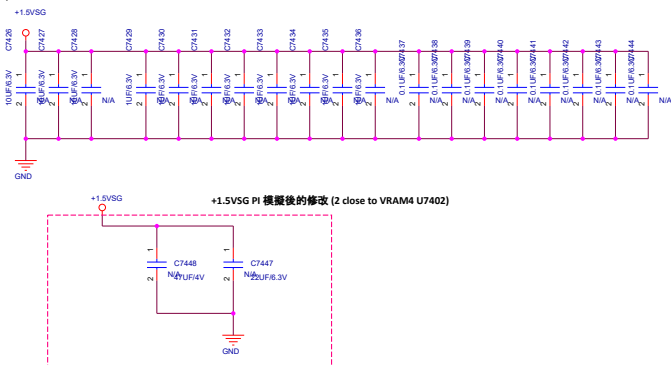
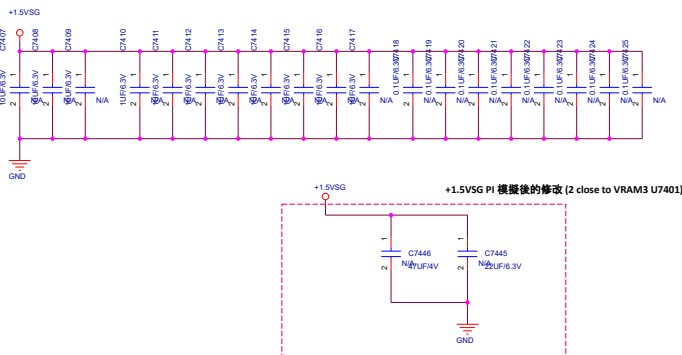
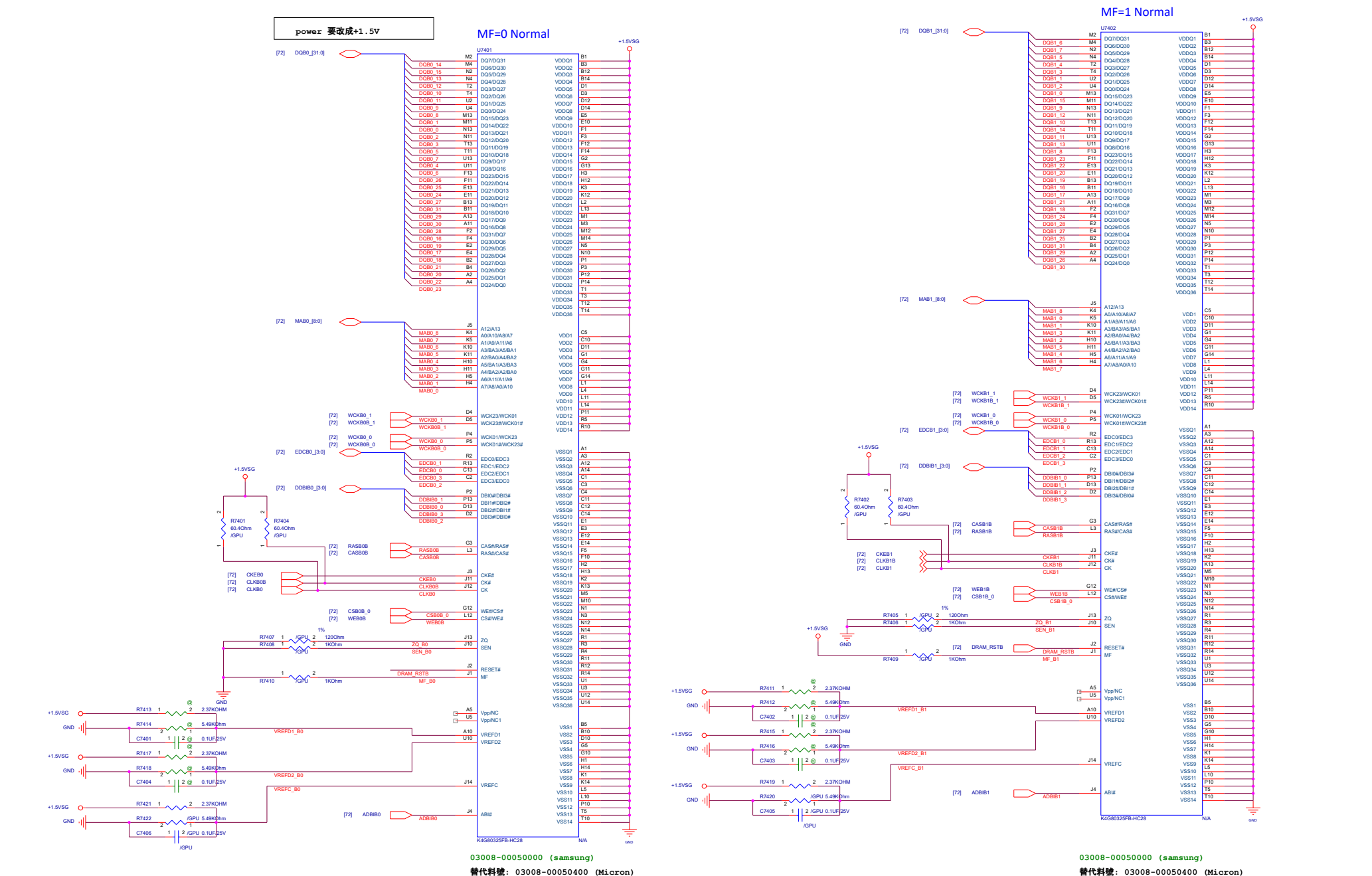
Component		ASUS P/N	Priority	品名	料番	Vendor
VRAM	99	0000-0000500	1	G5045 256M(12) 7E 1.5V FBGA1379	SAMSUNG/K4G680256H-HC38	Samsung
		0000-0000500	2	G5045 256M(12) 7E 1.5V FBGA1379	MBROCN/MT1251256M12M1-70DA	Microson
	20	0000-0000100	1	E6000 128M(8) 7E 1.5V BGA1179	HYUNDAI/HY64648128AHC-PC2	Hyundai
		0000-0000100	2	OC600 128M(8) 7E 1.5V BGA1179	SAMSUNG/K4G401252H-PC2	Samsung





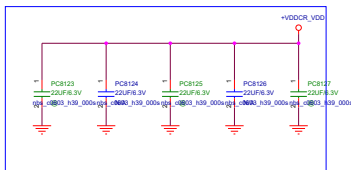
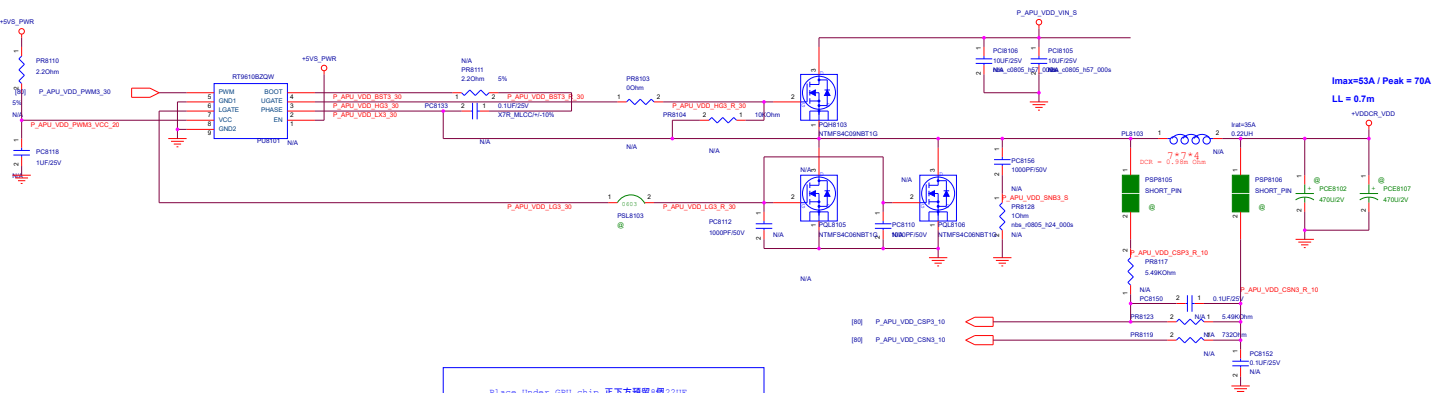
Load Switch

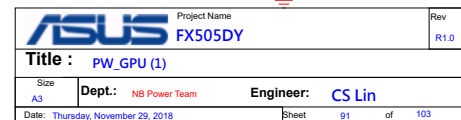




GDDR5 256x32_7.0G (8Gb)

Priority	Company	Model Name	Base	Voltage	Speed	MP Schedule	ASUS P/N
1	Samsung	K4G80325FB-HC28	Samsung	256x32	1.35V/1.55V	6.0G/7.0G	03008-00050000
2	Micron	MT51J256M32HF-70:A	Micron	256x32	1.35V/1.5V	6.0G/7.0G	03008-00050400

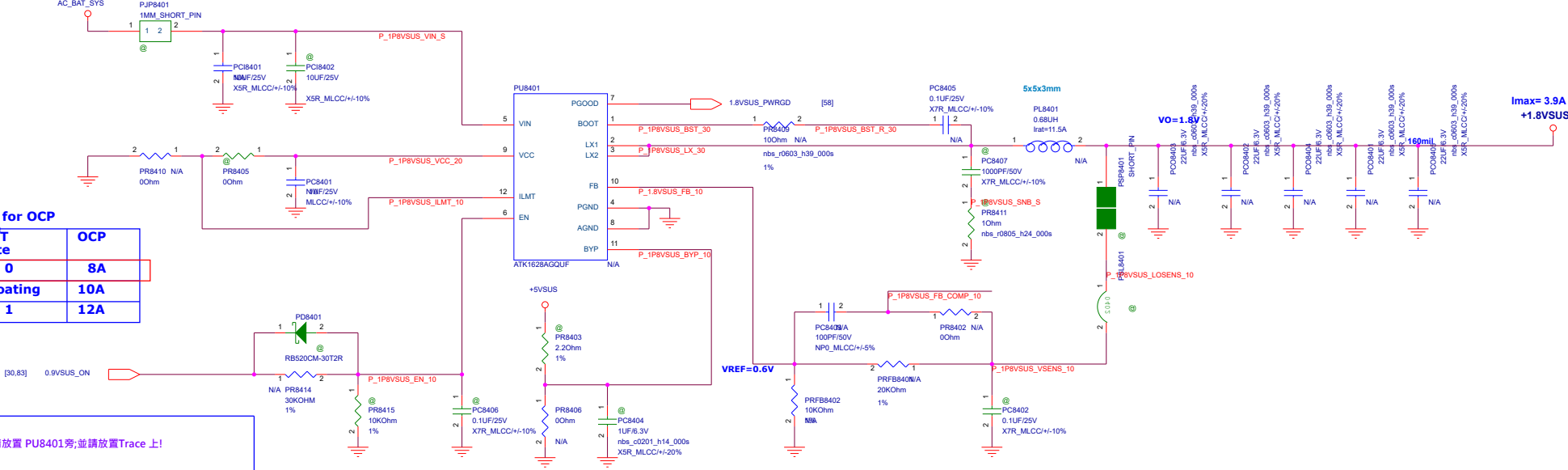




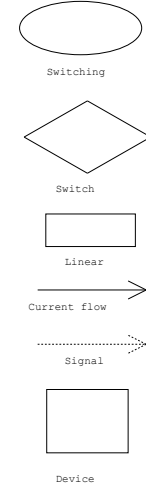
ILMT for OCP


ILMT State	OCP
0	8A
Floating	10A
1	12A

PT840* 請放置 PU8401旁;並請放置Trace 上!



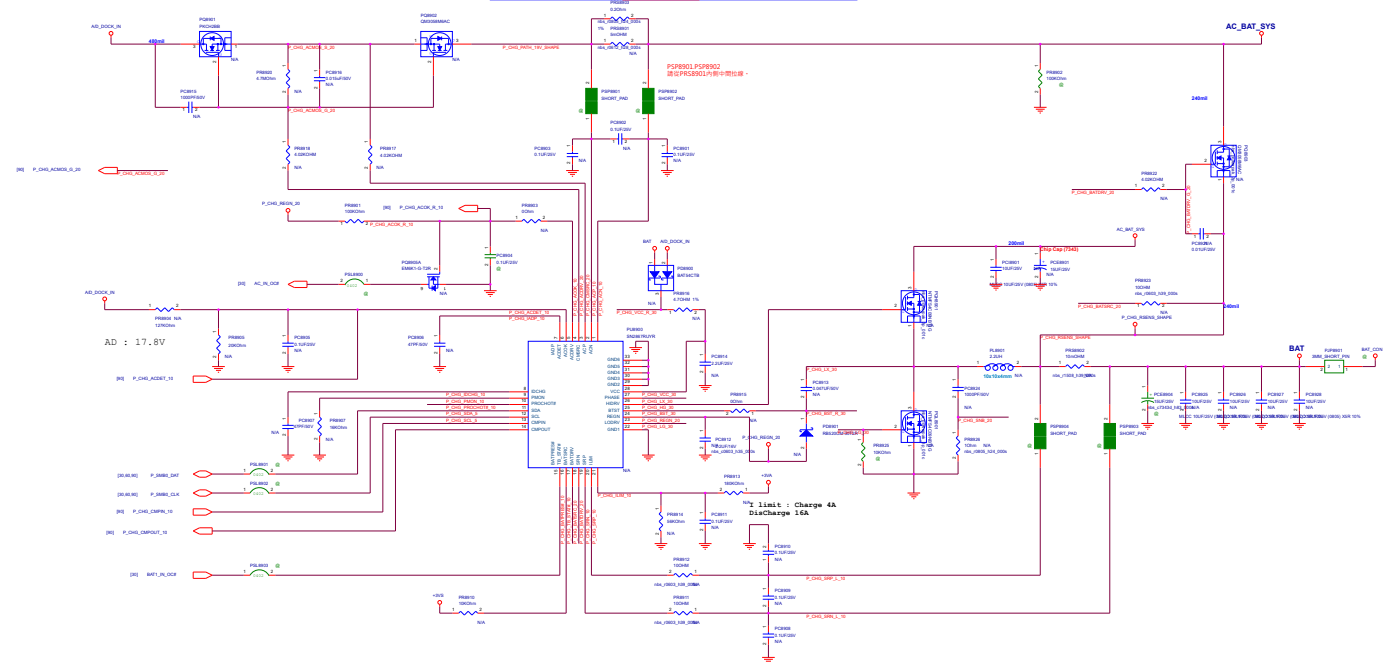
<Variant Name>



		Project Name	Rev
		FX505DY	R1.0
Title : AMD_CPU_GND			
Size B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3		
Date: Thursday, November 29, 2018	Sheet	102	of 103

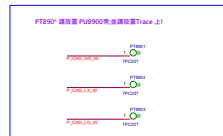
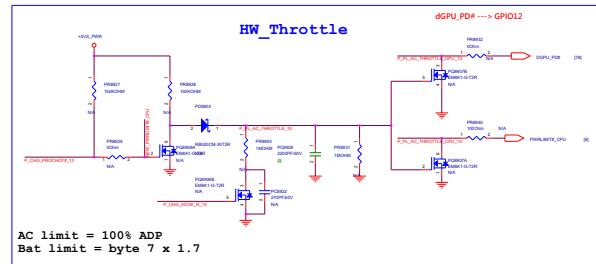
P88903	ADP<150W	ADP=150W	ADP=180W	ADP=230W	ADP=330W
	200m	255m	X	X	X
	1001A-00010001	1001A-00020000	X	X	1001A-00010001

P88901	<=150W	<=280W	>280W	>330W
	10m	5m	5m	2m
	1000A-00010001	1000A-00000000	1000A-00000000	1000A-00000000



Adaptor select
total power = 90% ADP

Adaptor select				
	W	Resistor	W	Resistor
P88921	10m	5m		
P88936				
14K	0.4V	30W	120W	
31.6K	0.8V	40W	150W	
56K	1.2V	45W	180W	
93.1K	1.6V	65W	230W	
150K	2.0V	75W	280W	
270K	2.4V	90W	330W	
560K	2.8V	120W	400W	



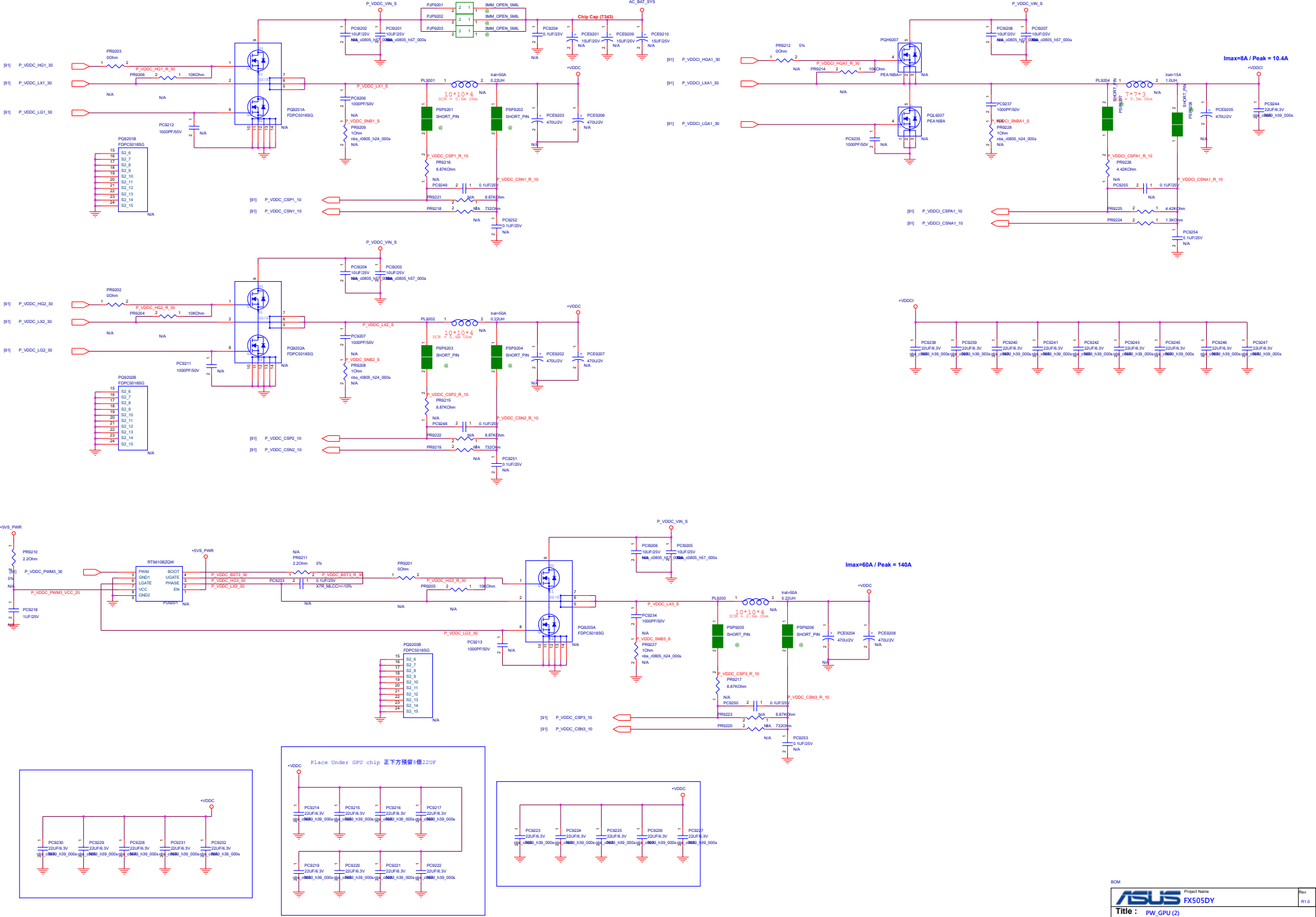
ASUS		Project Name	
FX505DY		File	
PK CHARGER		Rev	0.1
Date		Engineer	CS Lin
Drawn		Check	
Date		Draw	

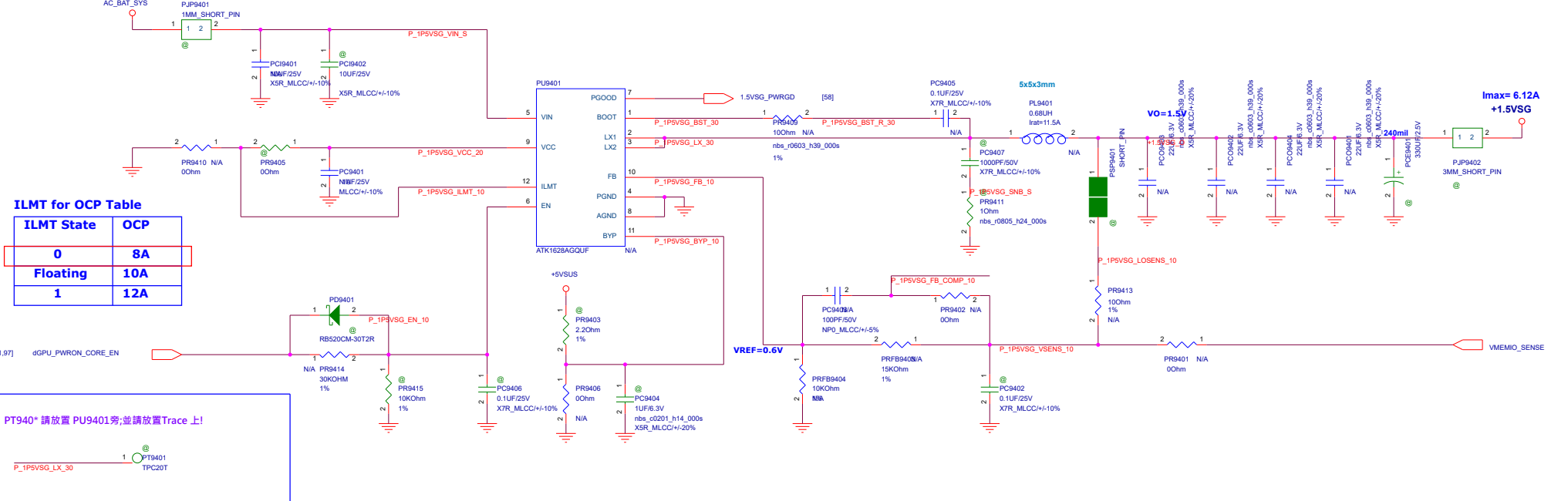
Address	Q ₆₇	Q _{67C}	Q _{67A}	Q _{67B}	Q _{67E}	Q _{67D}	Q _{67S}	Q _{67O}
PR5101	10h	1.0h	2h	3.0h	3.0h	4.0h	5.1h	6h
PR5103	000h	8.1h	8.1h	8.8h	4.7h	3.0h	2.7h	2h

Register Address							
Address	SeD3	SeD1	SeD2	SeD3	SeD2	SeD1	SeD0
0x0	R	R	R	R	R	R	R
Function	Temp. alarm threshold setting			Second temp. data			bit 0 = 0 bit 1 = 0 bit 2 = 0 When ALERT2 occurs

[illegible][illegible]

PR9050 set OCp:
 loop(A)=1000/(ACFET_Rdson(mOhm)*PR9050/(Kohm))
 design loop = < 1.2*ACFET_Iconst (10ms latch)
 1.5*loop (latch immediately)
 Design precaution: loop must not trigger Adapter 200% protection
 EX: use 280W ACFET-QM3053BM6AC(21A cont.)
 loop design at 21A*1.2=25.2A ==> 1.5*loop=37.8A
 1.5*loop > Adapter 200% rating



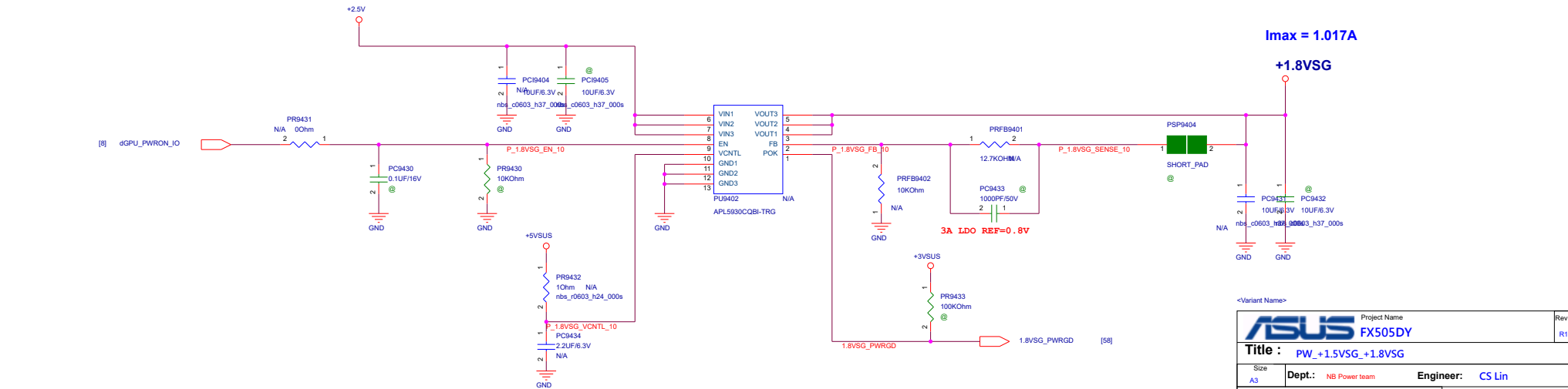


ILMT for OCP Table

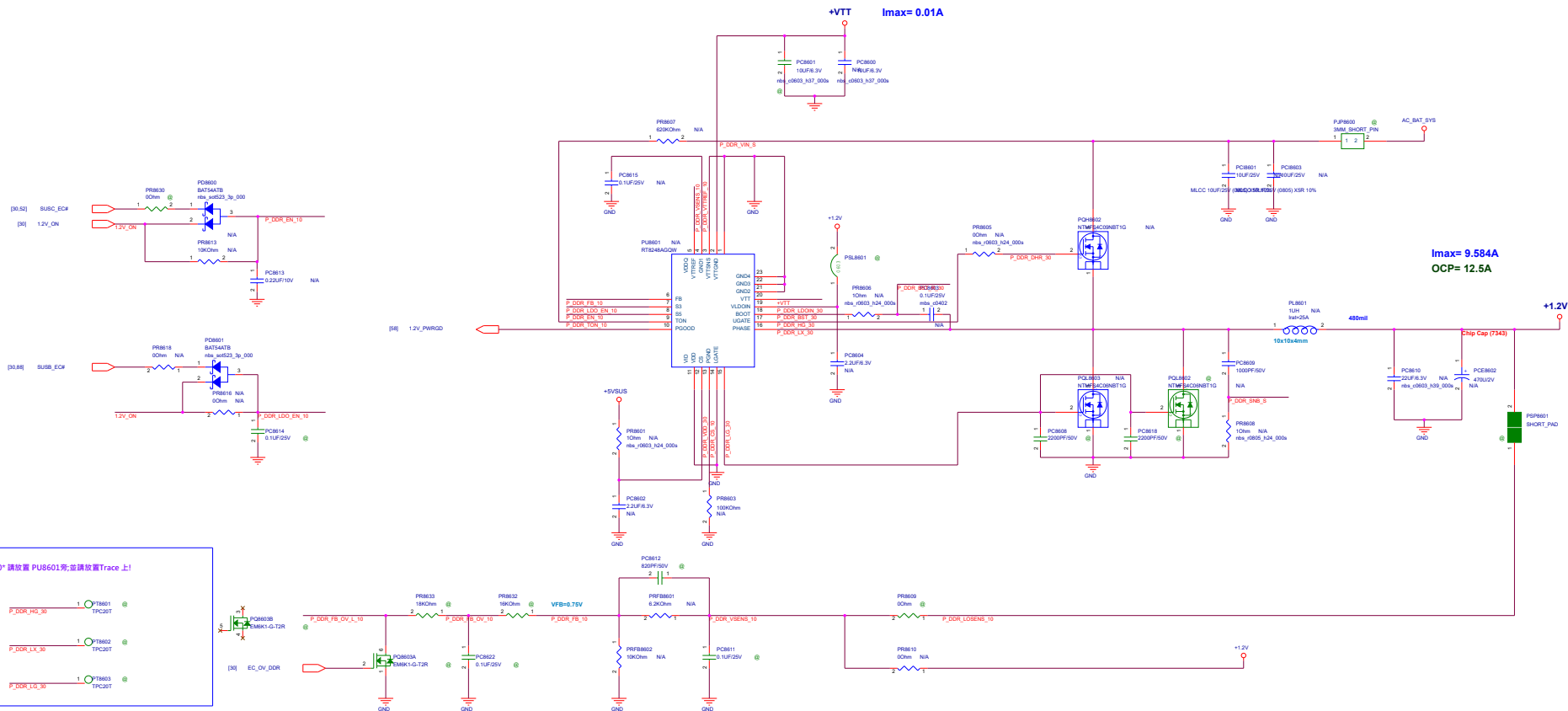
ILMT State	OCP
0	8A
Floating	10A
1	12A

PT940* 請放置 PU9401旁;並請放置Trace上!

P_1PSVSG_LX_30




+1.2V / +VTT / +2.5V[For Memory]



~Core Design~

Project Name		Rev
FX505DY		R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size	Dept.: NB Power team	Engineer: CS Lin
Date: Thursday, November 20, 2015	Sheet	88 of 103

		Project Name	Rev
		FX505DY	R1.0
Title : AMD_CPU_GND			
Size			
B	Dept.:	ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date:	Thursday, November 29, 2018	Sheet	103 of 103